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Towards Runtime Adaptivity by using Models of Computation for Real-Time Embedded Systems Design

D. S. Loubach ¹ E. G. O. Nóbrega ¹ I. Sander ² I. Söderquist ³ O. Saotome ⁴

¹University of Campinas - UNICAMP

²KTH Royal Institute of Technology

³Aeronautics, Saab AB

⁴Aeronautics Institute of Technology - ITA





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- Reconfigurable computing
- Embedded systems
- Real time systems
- Real time operating systems
- Model-based design

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Motivation: aeronautics current trend towards the second generation of **integrated modular avionics** (IMA2G), a.k.a. distributed IMA

Our paper shows that **runtime adaptivity** is feasible to be performed

Case study implementation on both software and hardware, using a **heterogeneous SoC** (uC + FPGA)

To capture and deal with the complexity of adaptivity, we modeled a case study using the theory of **formal models of computation** (MoC), mainly the synchronous MoC



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Model of Computation (MoC)

- Event, Signal, Process
- Synchronous MoC
- ForSyDe
- Real-time embedded systems
- Adaptivity
 - Full vs. Partial reconfiguration

- Modeling of adaptivity
 - Signals carrying functions
 - Adaptive process



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Figure: Process constructor for *reconfigSY* adaptive process

$$ap_f = reconfigSY_n$$

 $o = ap_f(s_f, (i_1, \dots, i_n))$ $o[k] = s_f[k](i_1[k], \dots, i_n[k])$

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Processes definitions:

$$genEncoder: s_f[k](s_{key}[k]) = s_{encF}[k]$$
(1)

$$ap_{encoder}: s_{encF}[k](s_{input}[k]) = s_{enc}[k]$$
(2)

$$genDecoder: s_{f^{-1}}[k](s_{key}[k]) = s_{decF}[k]$$
(3)

$$ap_{decoder}: s_{decF}[k](s_{enc}[k]) = s_{output}[k]$$
(4)

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Figure: SoC with the ProgDev and ReconDev areas overview. It also contains the ReMan software application inside the ProgDev



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Signals containing the encoding and decoding functions:

$$s_f = \langle (enc_{AES}), (enc_{DES}), \ldots \rangle$$

 $s_f^{-1} = \langle (dec_{AES}), (dec_{DES}), \ldots \rangle$

$$s_{f}$$
 and s_{f}^{-1} signals turned in $s_{f'}$ (for simplicity):
 $s_{f'} = \langle (f_{AES}), (f_{DES}), \ldots \rangle$ (5)

where:

 f_{AES} stands for AES cryptography (encoder/decoder) function;

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 and s_f^{-1} signals turned in $s_{f'}$ (for simplicity):
 $s_{f'} = \langle (f_{AES}), (f_{DES}), \ldots \rangle$
(5)

where:

 f_{AES} stands for AES cryptography (encoder/decoder) function;

 f_{DES} for the DES cryptography (encoder/decoder) function







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- ReconDev clock: 50 MHz (20 nano seconds period)
- ProgDev clock: 925 MHz

Table: Functions and sub functions runtime clock cycles and computation time

Main function	Sub function	Clock cycles	Time [ns]
f_{AES}	encode	63	1,260
<i>f</i> _{AES}	decode	63	1,260
f_{DES}	encode	18	360
f_{DES}	decode	19	380



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Partial and full reconfigurations

Table: Partial reconfiguration measured times. (*)Time is given in mili seconds [ms]

Bitstream mode	prosopon _{AES} *	prosopon _{DES} *
Scrub	7.76	7.76
And/or	12.7	12.4

Table: Full reconfiguration with no data compression measured time. (*)Time is given in mili seconds [ms]

Bitstream	Time*
FR	29.6



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Ack. Q&A We introduce in this paper a **runtime adaptivity case study** using **formal models of computation** (MoC) for real-time embedded systems design

We modeled an encoder/decoder system in a high-level of abstraction (*system specification*) using ForSyDe

Next, we refined that model and manually transformed it into an *implementation specification* to be designed in software/hardware



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Results showed that one partial reconfiguration takes less time to complete than a full reconfiguration

This enables the possibility to **runtime reconfiguration using partial reconfiguration techniques**, then leading to runtime adaptivity feasibility



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