Single-Event Upset Detector Based on COTS FPGA

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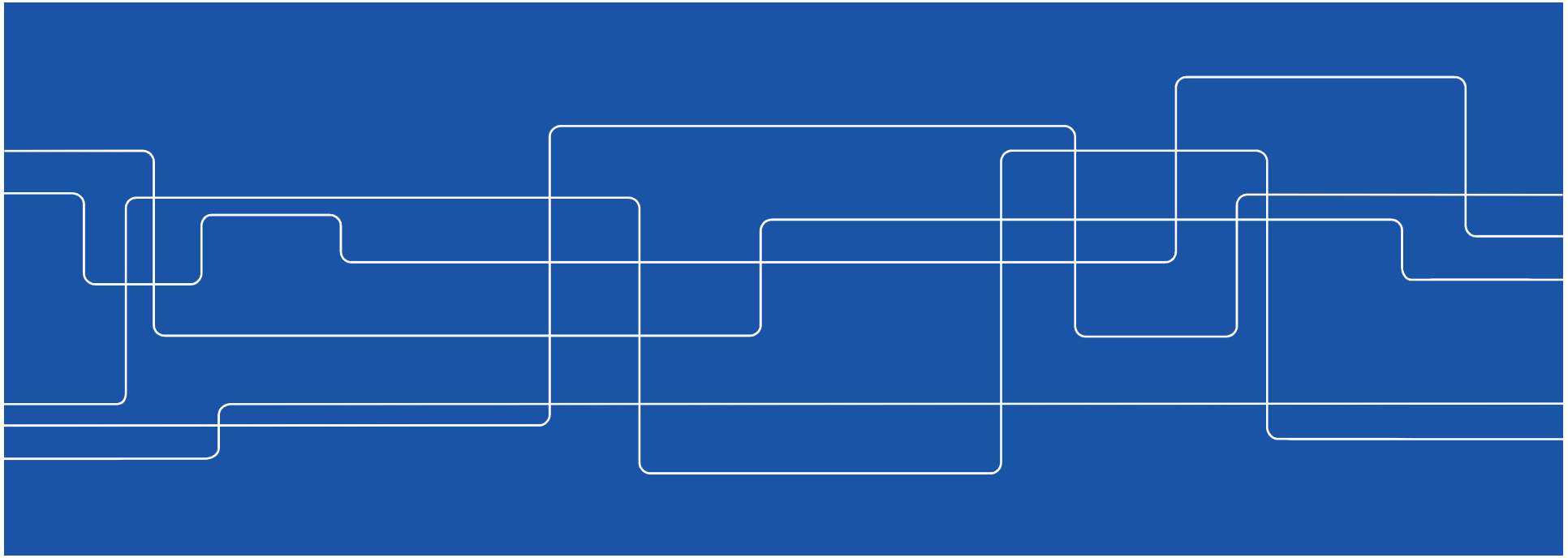
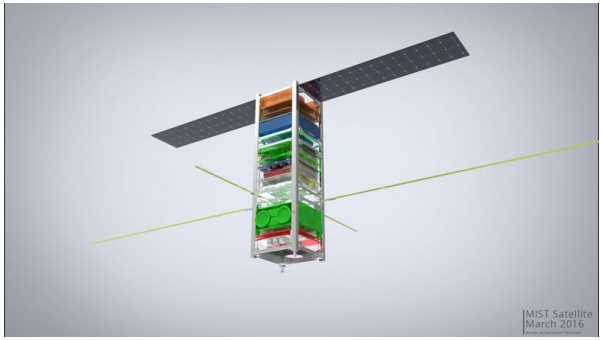
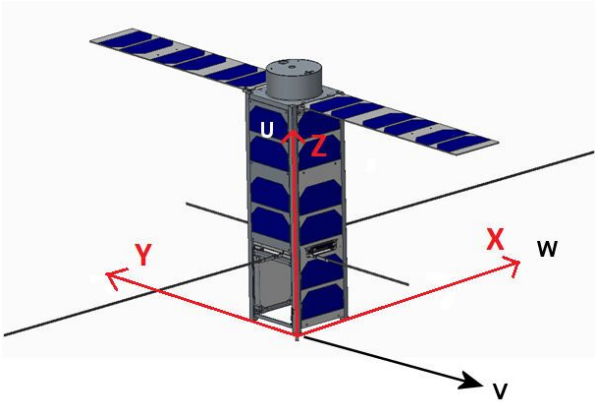


MIST – MIniature STudent satellite





1)	CubeProp	-	NanoSpace AB, Uppsala
2)	RATEX-J	-	Inst. Space Physics, Kiruna
3)	Piezo Legs	-	Piezomotor AB, Uppsala
4)	CUBES	-	Space Physics, KTH
5)	SiCs in Space	-	EKT, KTH
6)	MoreBac	-	BioTechnology, KTH
7)	SEUD	-	ESY, KTH
8)	OBC	-	SCS, KTH
9)	Camera Unit	-	ESY, KTH

SEUD – Single-Event Upset Detector

Three-fold experiment:

1) Use COTS FPGAs in Space
2) Counting Single-Event Upsets in an Hostile Environment
3) Safe execution of functionality in presence of SEU:s

    a) Triple-Modular Redundancy in HW
    b) Duplication of functionality in SW
    c) Healing Core for Soft-Error Mitigation

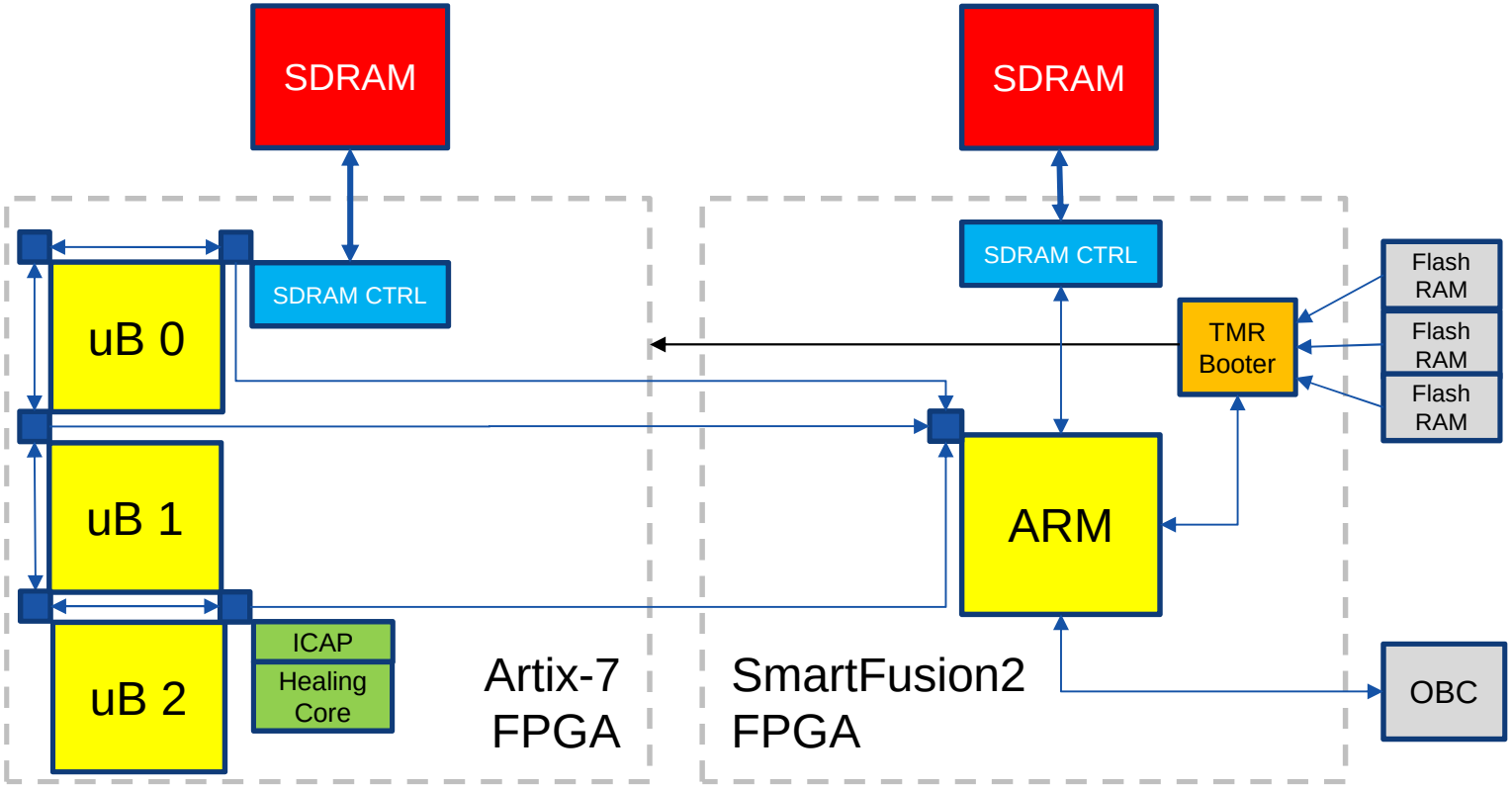
Soft-Errors in FPGAs

1) SET – Single Event Transients
   - Voltage spikes on wires

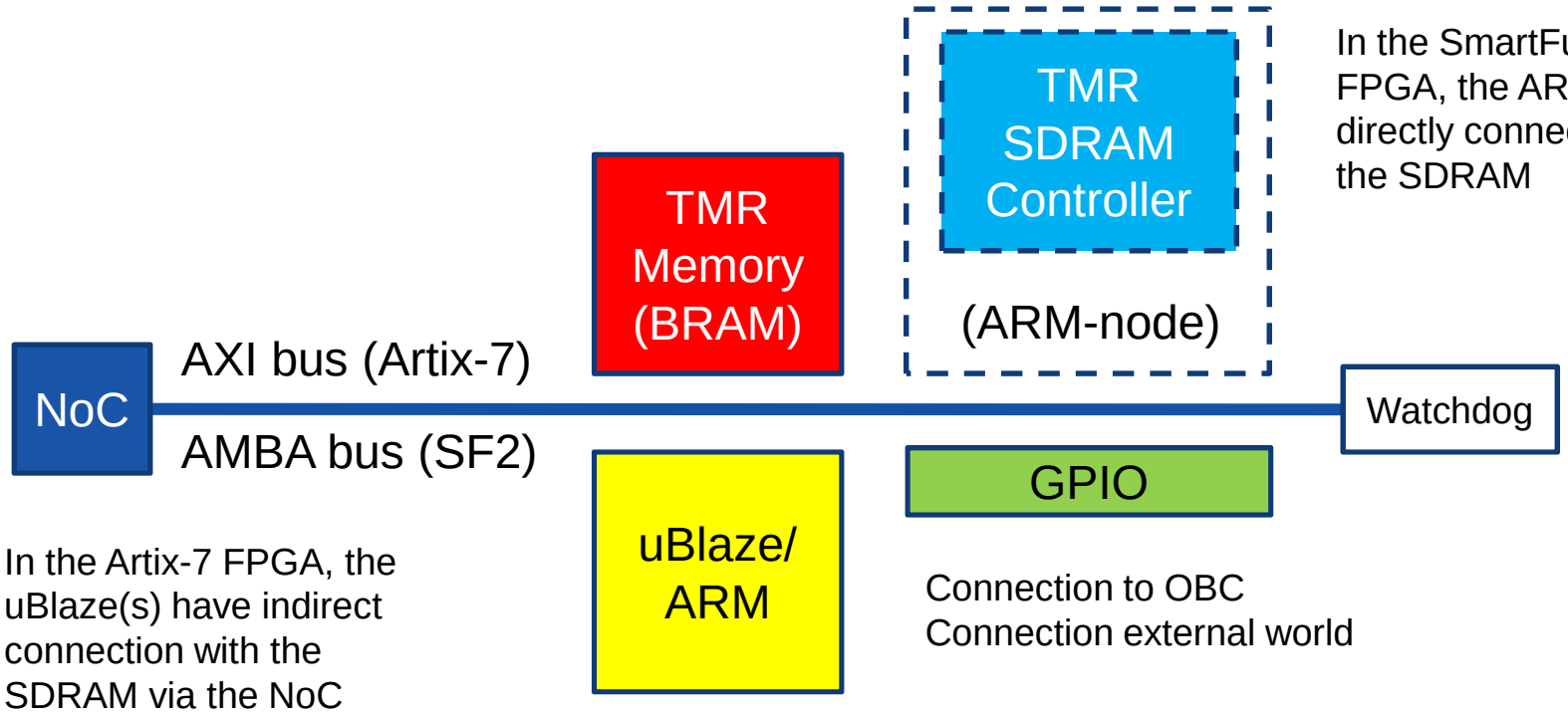
2) SEFI – Single Event Function Interrupts
   - Configuration Memory bit flips

3) SEUs – Single Event Upsets
   - RAM or Flip-flop bit flip

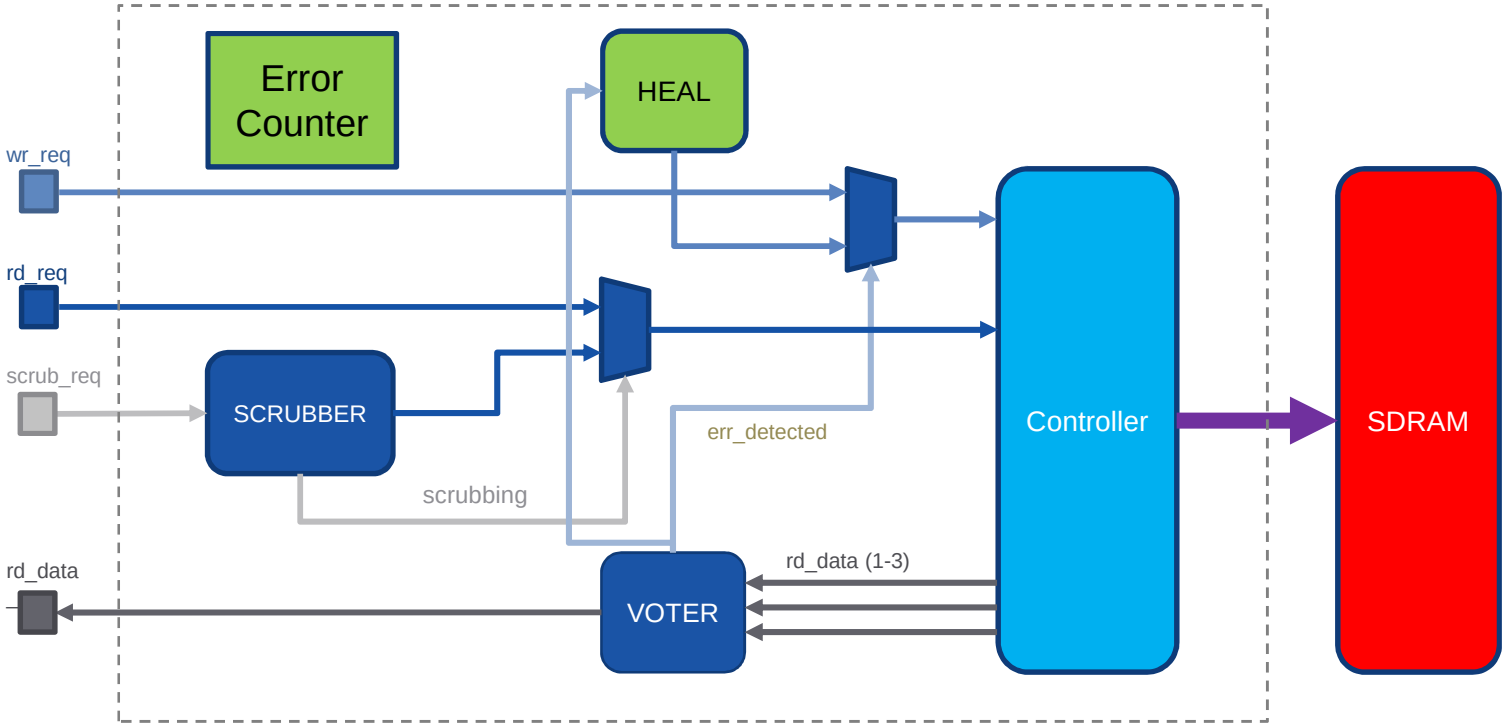
Overall Architecture



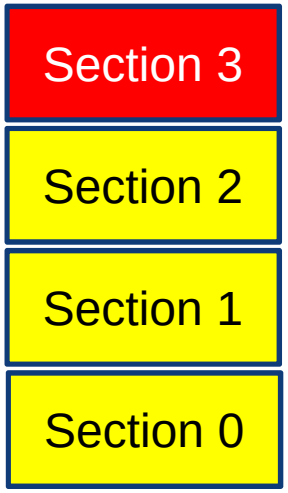
MicroBlaze/ARM node



SDRAM Controller



SDRAM Memory Layout



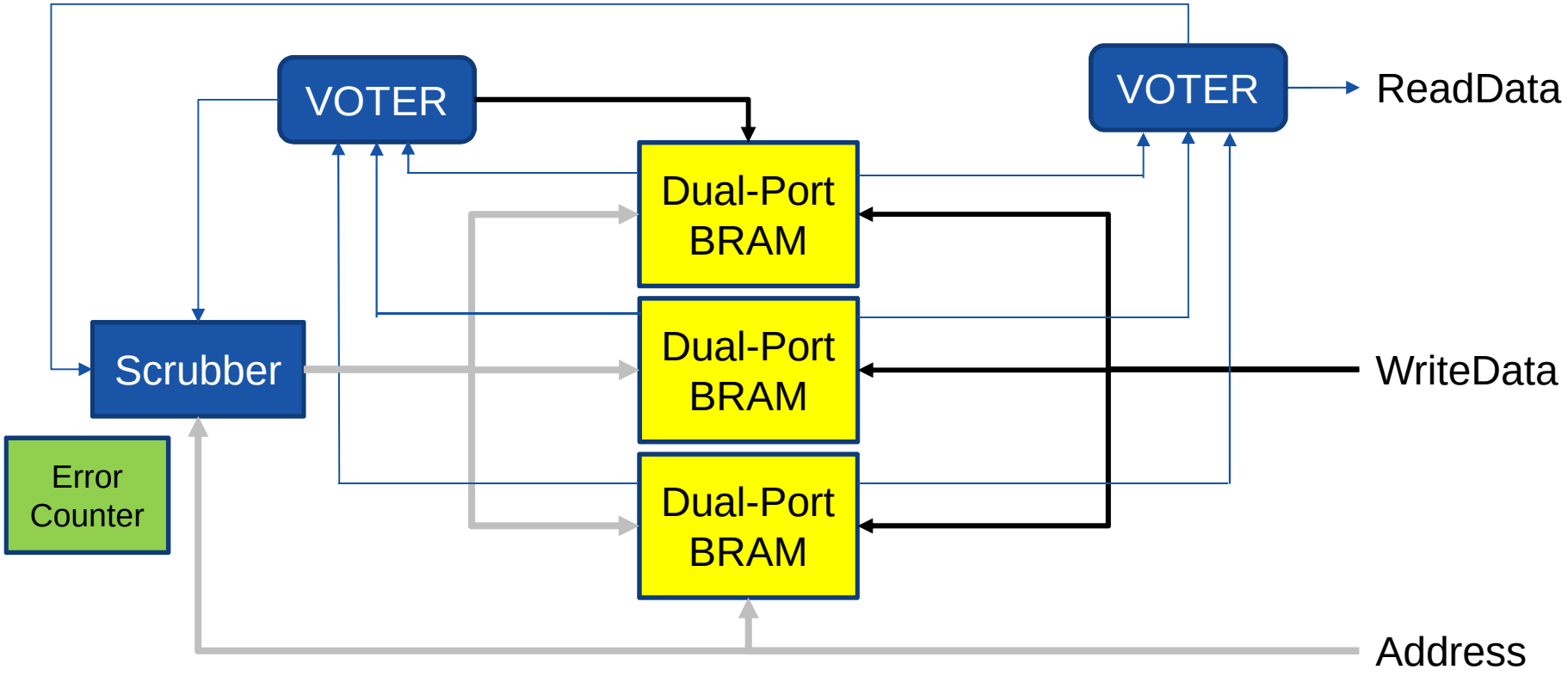
Each Row is divided into four sections
- Three sections form a TMR memory
- One section works as normal

1) Data and Code that needs protection is stored in the TMR sections.
(Program Code and Configuration data)

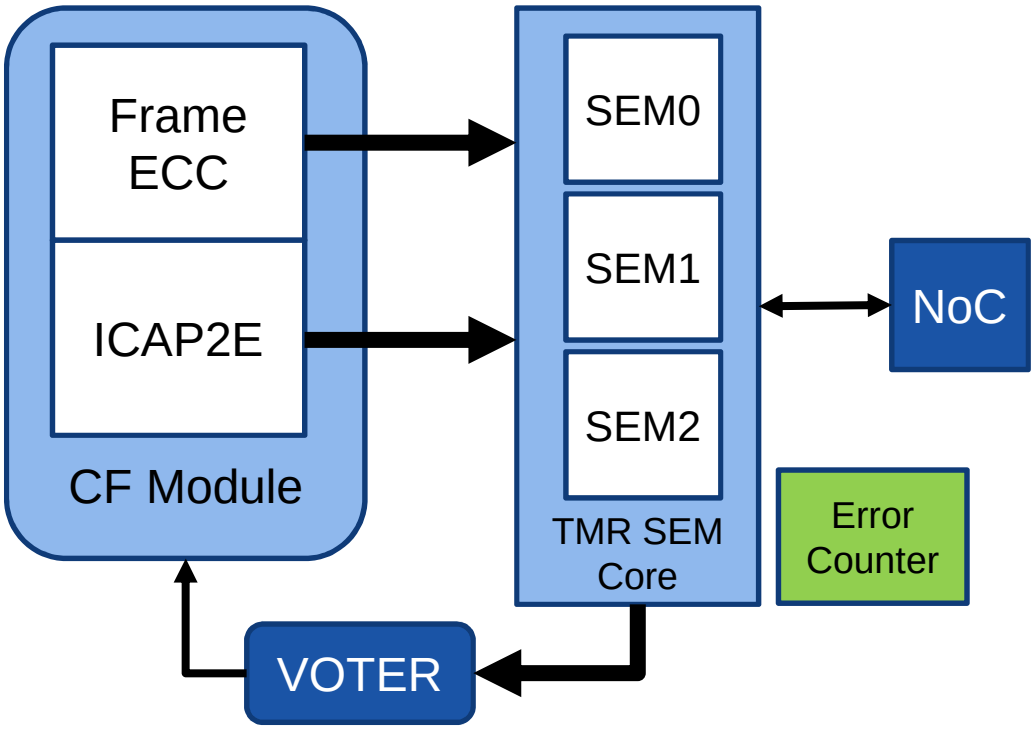
2) The normal section is filled with a known pattern for SEU Detection.

3) Errors are counted and stored in a special register inside the SDRAM controller.

BRAM TMR Memory

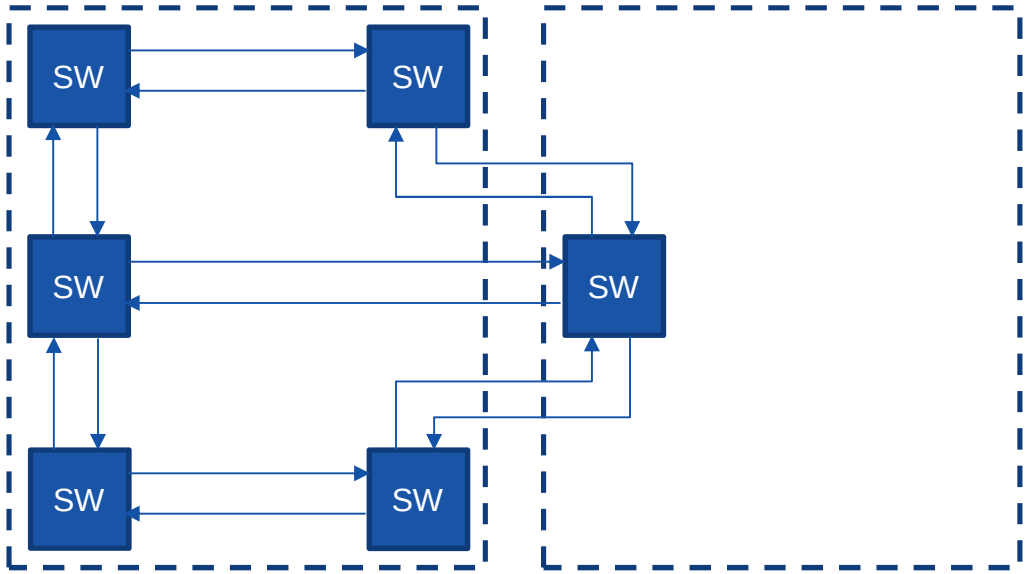


Healing Core



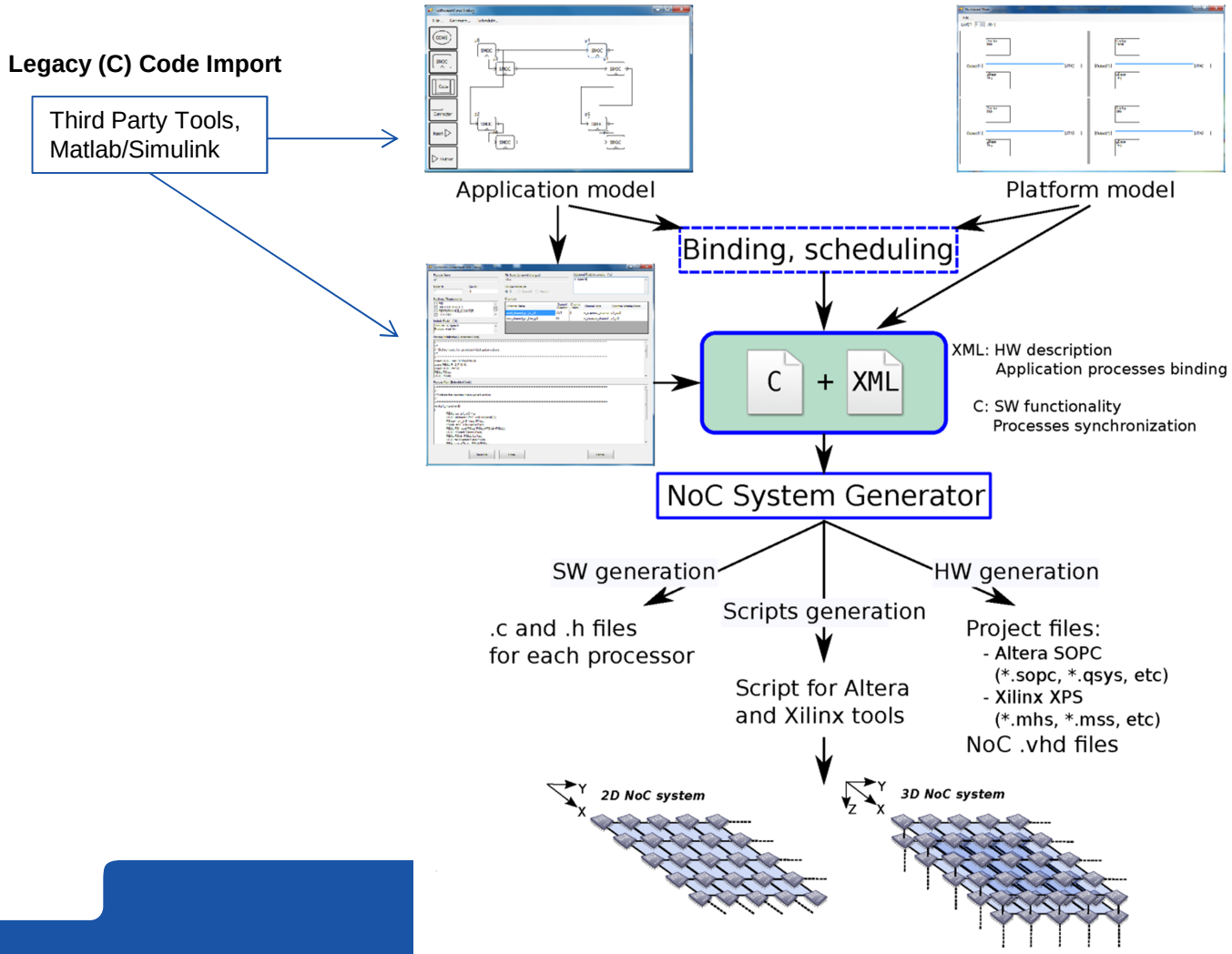
1) Correct faults using the SEM units
2) If it exceeds ECC's capabilities, initiate partial reconfiguration:
   a) Get data from SDRAM
   b) If SDRAM controller is compromised, retrieve Golden-Copy from TMR Flash

Network-on-Chip

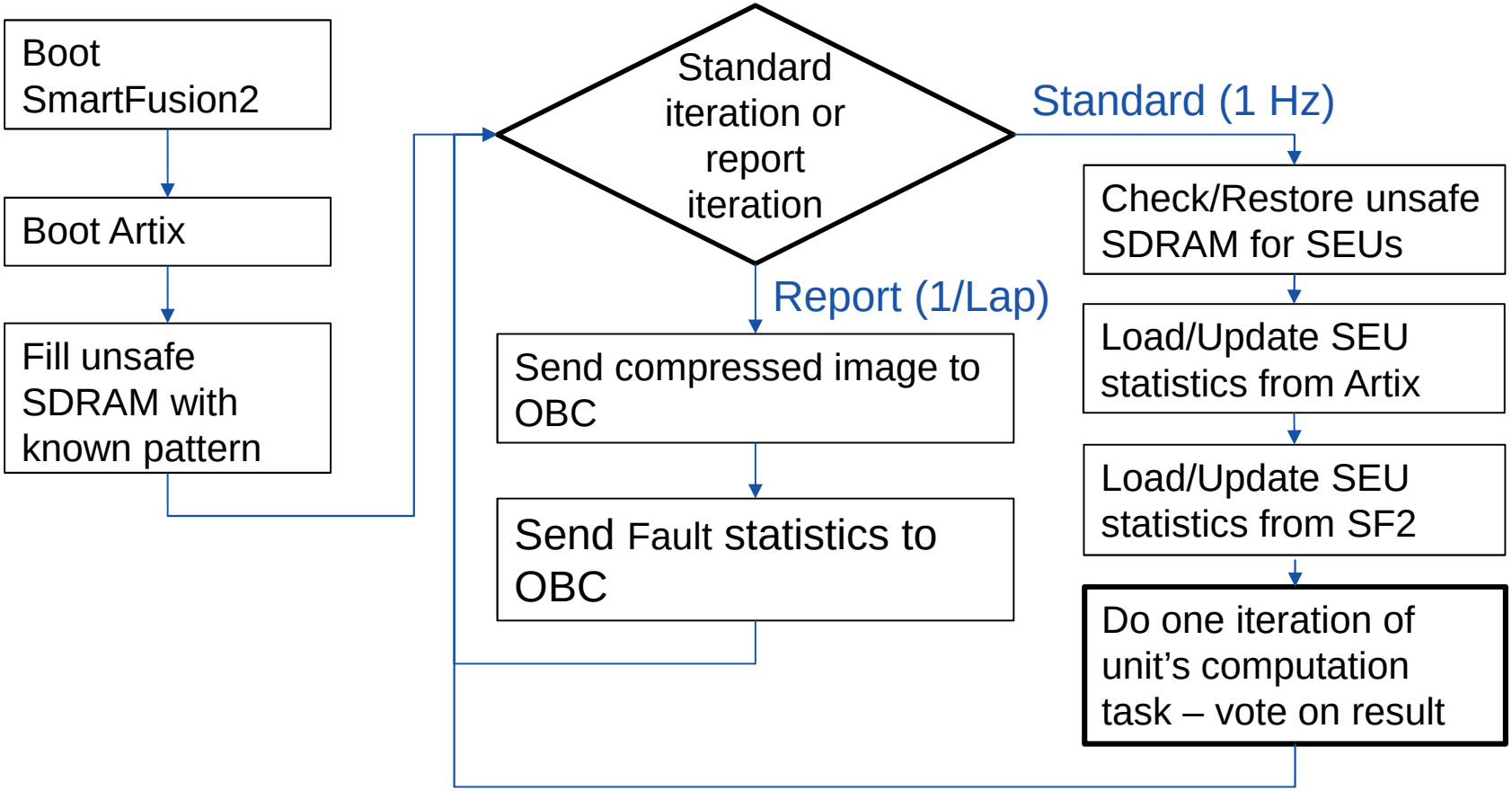


1) 2x3 NoC
2) Nostrum NoC with Guaranteed Service using TDNs
3) Dual unidirectional links between nodes
4) MPI-based communication between nodes
5) 6 Mesochronous clock bridge(s) between Artix and SF2 FPGAs
6) Faulty flits in the messages are dropped in the switches.
7) Missing flits in messages are detected by the SW.

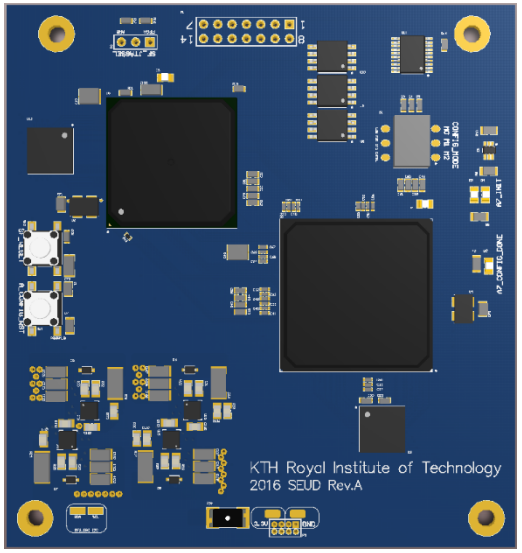
NoC System Generator



Overall SW Architecture



Results



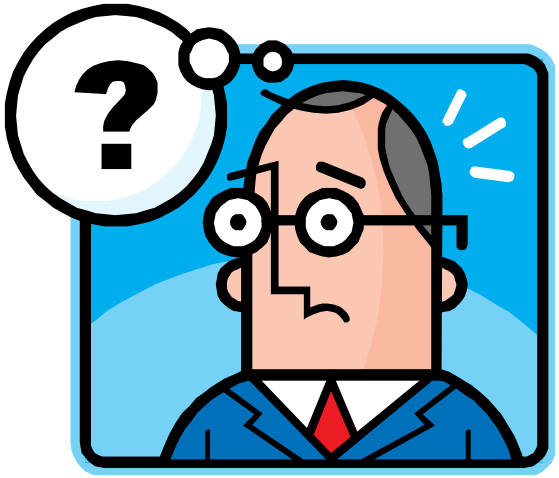
Current Status

- PCB Manufactured – currently ordering components
- Partial Prototype Implementation up and running on Nexys Video Artix-7 board
  - ✓ Healing Core implemented and tested
  - ✓ Run-Time Correction implemented and tested (using Fault-injection)
  - ✓ SDRAM controller implemented and tested on Altera DE2 board

Future Work

- Adding Camera connector to SEUD board
- DSE of NoC communication between the Artix and SF2
- System Integration (HW and SW)
- Testing complete system in radiation chamber

Thanks for your attention!



More information on MIST: https://www.kth.se/en/sci/centra/rymdcenter