IMA Platform Computing Module based on Partial Reconfigurable FPGA

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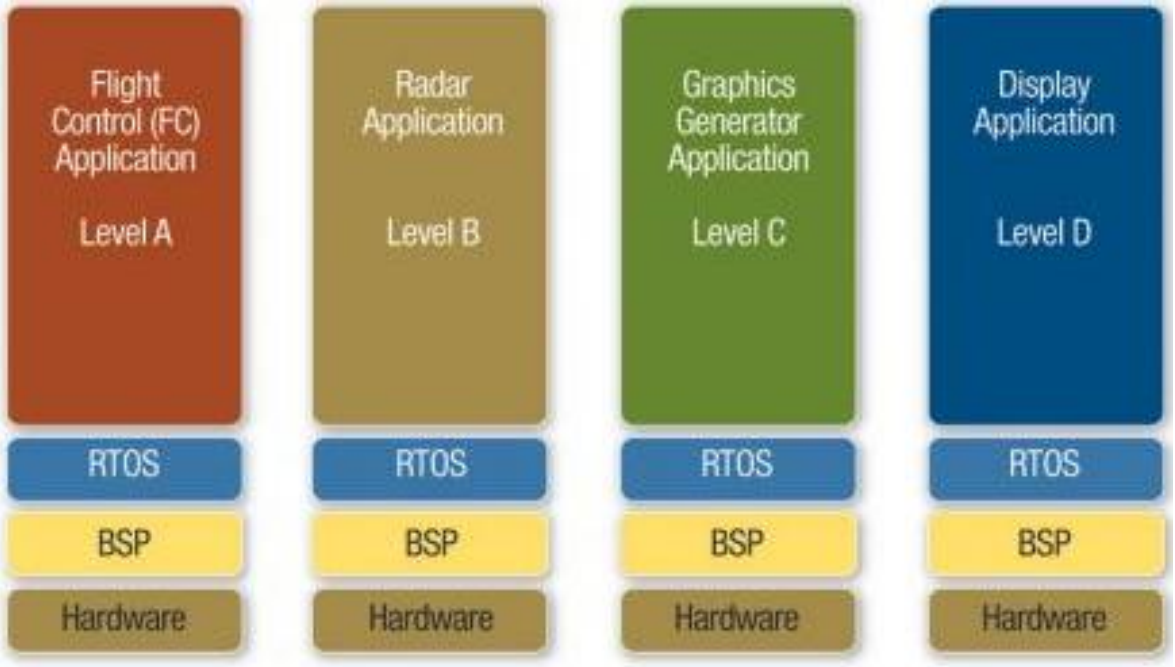
ABSTRACT

The present work proposes an IMA module design approach based on partial reconfigurable FPGA. The module can be able to exchange its internal behavior according to unexpected environmental changes or new application functionalities. The purposed approach allows a highly efficient hardware redundancy inside one chip itself, besides offering low-cost runtime reconfiguration feature.

INTRODUCTION

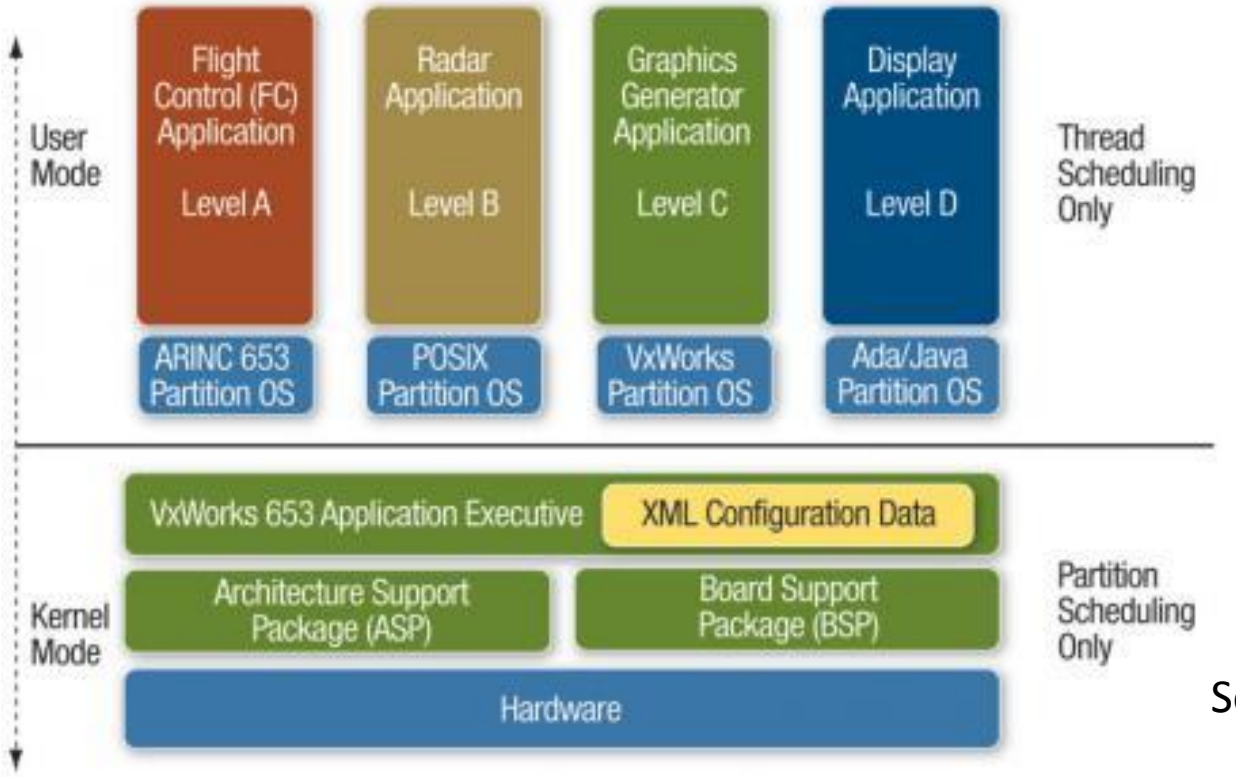
- Avionics systems are RTES (Real Time Embedded Systems) composed of processing modules and communication buses.
- They represent about 40 to 50% of aircraft cost (Bierber, et. al, 2007).
- In the past, avionic systems were based on **Federated architecture**.



Source: COTS Journal, July 2010.

INTRODUCTION

- **Integrated Modular Avionics (IMA)**:
  - Integrate multiple software functions with different criticality levels;
  - Strict and robust partitioning
  - Pros: integration, flexibility, interoperability, power, weight and cost reduction.



Source: COTS Journal, July 2010.

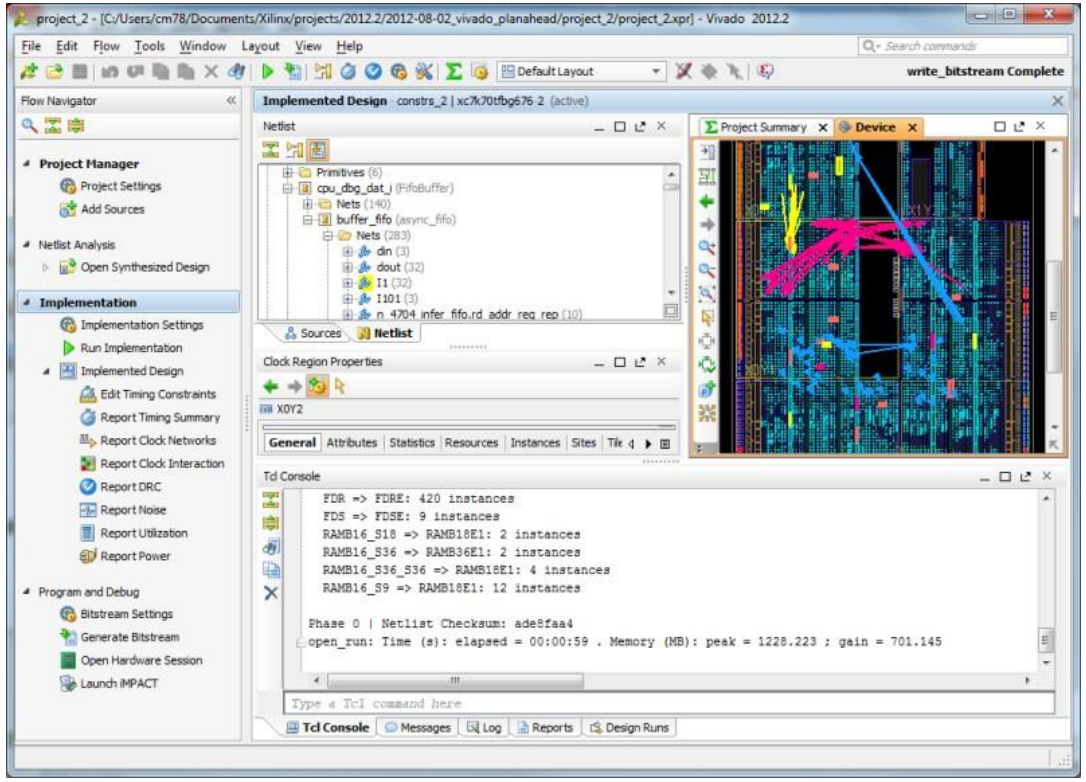
INTRODUCTION

- **IMA Second generation (IMA2G)**: realocation of functions to safe modules.
- **Field Programmable Gate Arrays (FPGAs)** are a possible hardware solution due to partial reconfiguration functionality.

Xilinx Arttix-7 FPGA

Source: directindustry.com

Xilinx Vivado



PRACTICAL DESIGN APPROACH

Case study: simple avionic system

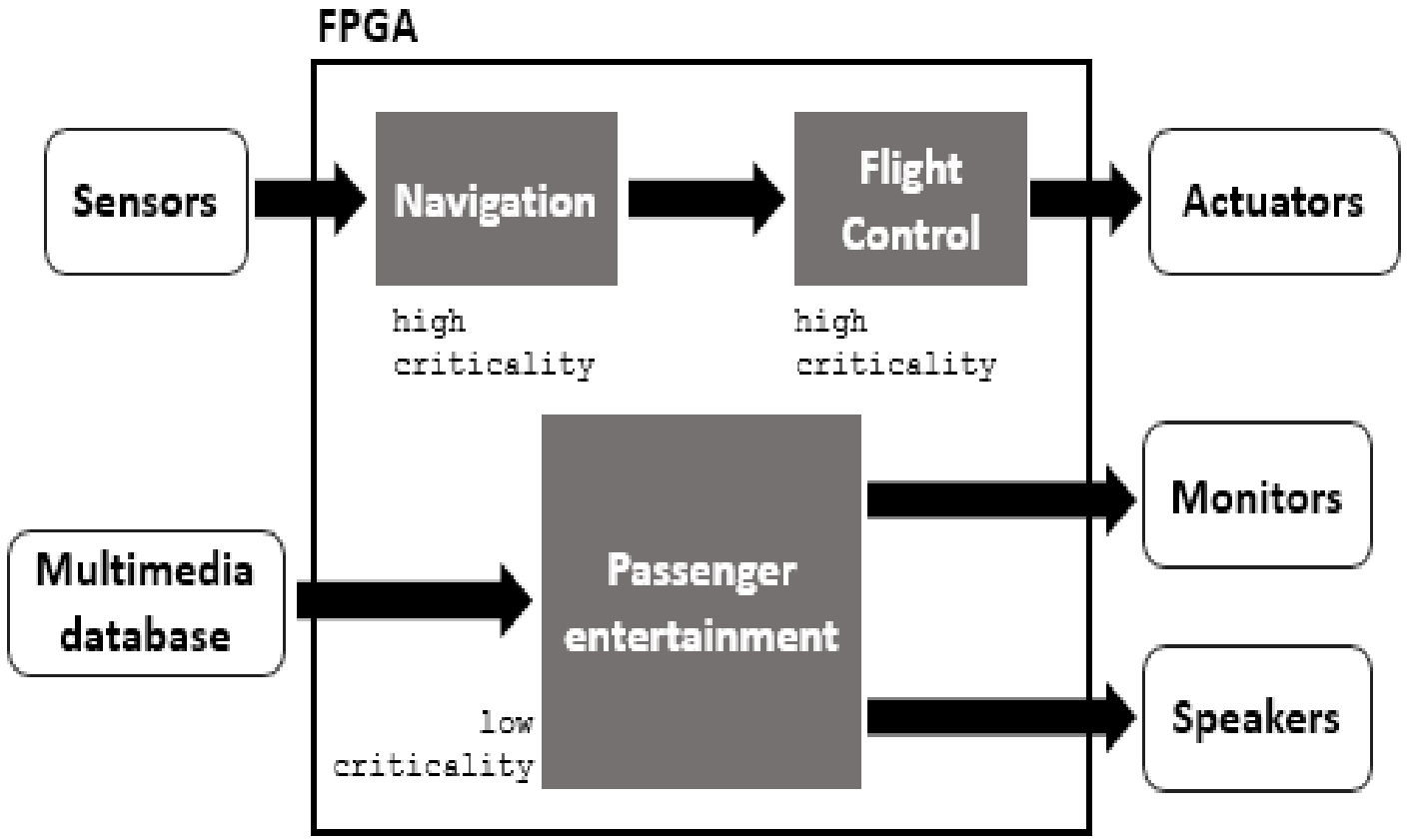
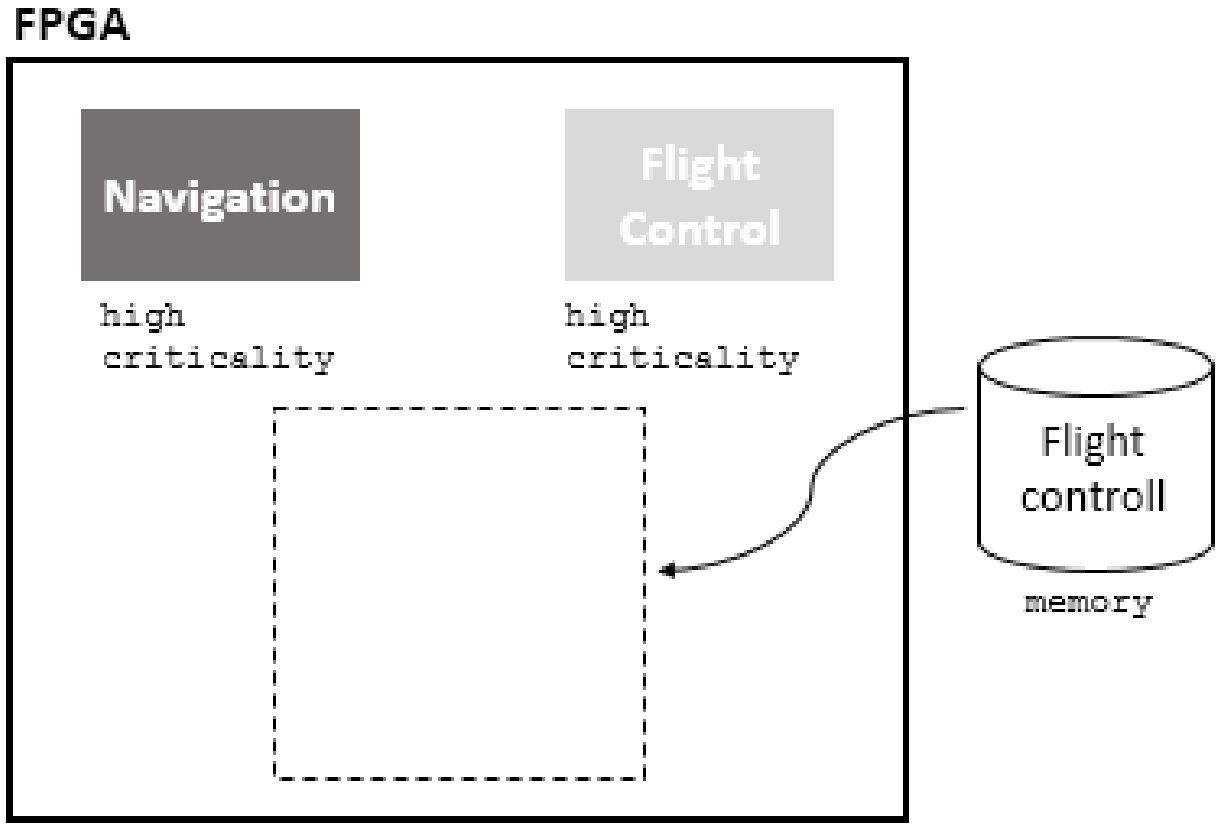


Fig. 1. Avionic system example

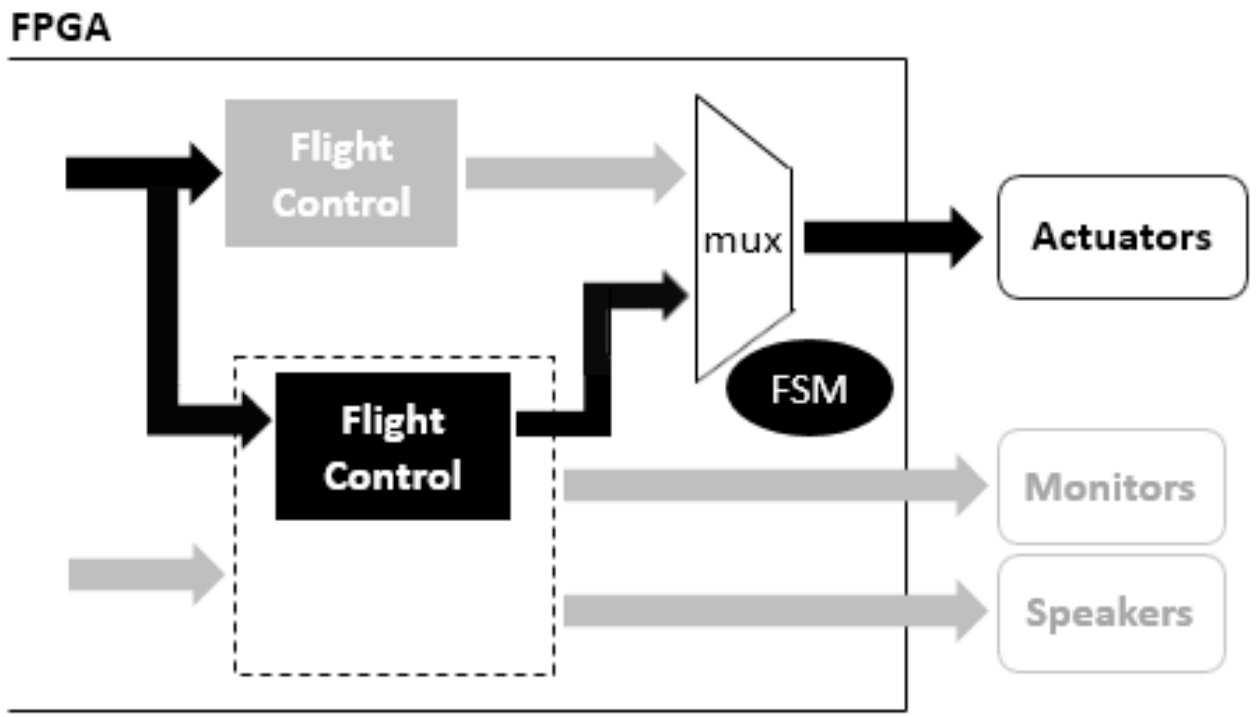
PRACTICAL DESIGN APPROACH

- **Step 1**: define superset entity/module



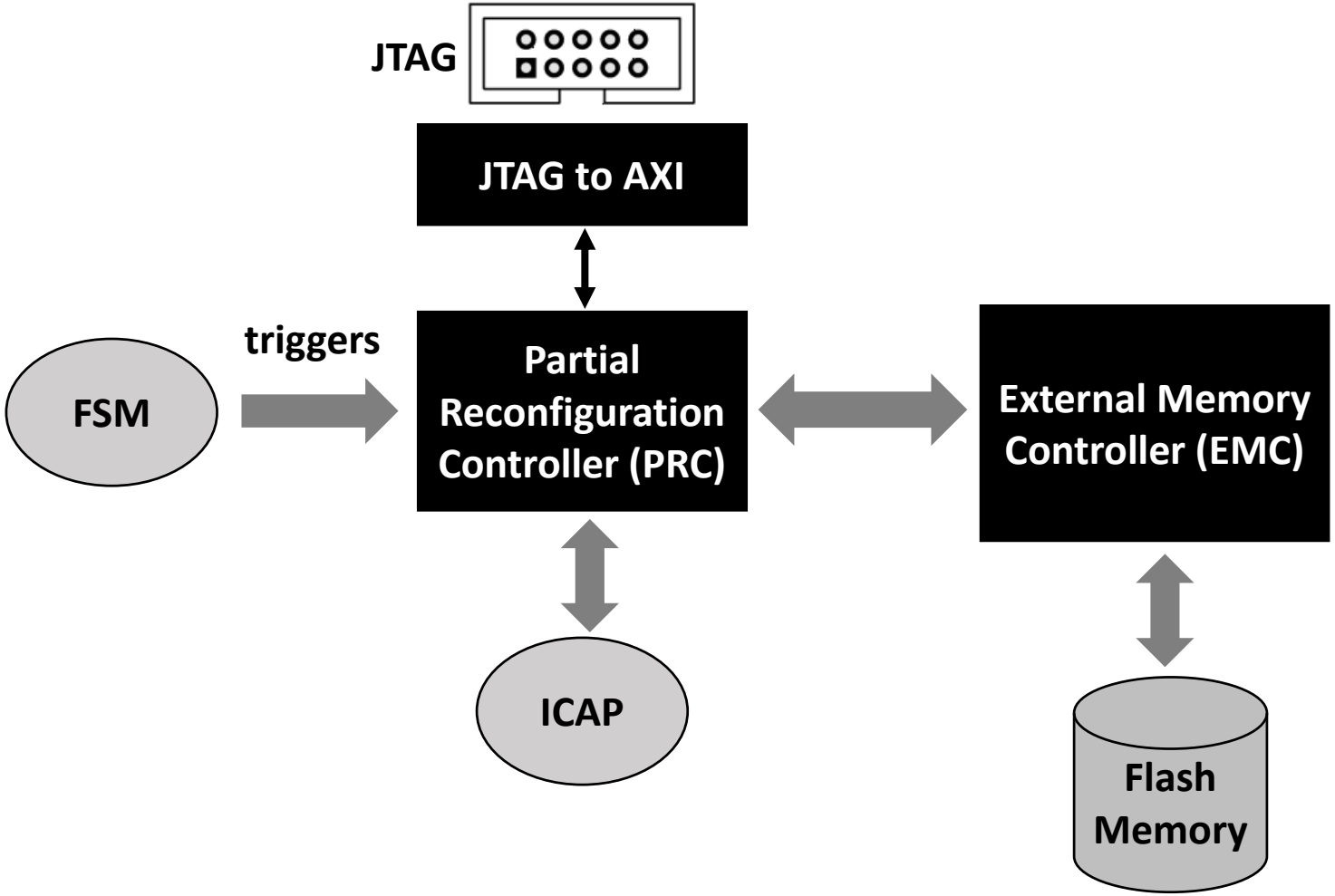
PRACTICAL DESIGN APPROACH

- **Step 2**: design finite state machine for mux control



PRACTICAL DESIGN APPROACH

- **Step 3**: generate out-of-context IPs



PRACTICAL DESIGN APPROACH

- **Step 4**: create top-level logic, run synthesis and implementation
  - Static + Reconfigurable Logic + FSM + IPs
  - Draw pblocks and save physical constraints
  - Synthesis and Implementation some possible configurations
- **Step 5**: generate bitstreams and update PRC
  - Each configuration = 1 full bitstream + *N* partial bitstreams
  - Calculate bitstreams addresses
  - Store full and partial bitstreams in flash memory
  - Update PRC via JTAG interface

CONCLUSION

The proposed design approach leads to on-chip run-time module reconfiguration, resulting in low cost, low volume and power reduction when compared with a conventional redundancy using hardware replication.

Our design approach can be adapted for other FPGA vendors, such as Altera, Lattice or Microsemi.

As future work, a real avionic system can be implemented through the purposed technique and performance indicators, such as power and reconfiguration time may be measured and compared with equivalent non-reconfigurable IMA

Thank you for your attention!

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