Real-time reconfiguration approach based on efficient classification and diagnosis of embedded systems

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Motivation

- There are several subjects to challenge current embedded hard real-time applications: Avionics is an example.
- High performance and flexible applicability are fundamental open issues.
- Fault-tolerant systems are mandatory, if there are human lives at risk.
- FPGA-based System-on-a-Chip (SoC) is today choice to develop real-time critical complex embedded systems, with fault-tolerance based on reconfigurability.
- A monitoring and diagnosis system shall be included with the ability to assess every system module, action, event or communication.

Proposed FDD

- A Fault Detection and Diagnosis (FDD) system is proposed, based on state estimation and assessment adopting classification methods
- The FDD proposed architecture provides a parallel framework that can achieve partial reconfiguration on real-time.
- A big data analysis based on multiple classifiers implementation, including rule-based, support vector machines and CNN.
- Preliminary tests shown high execution acceleration expected for the parallel implementation of the classifiers.

Current embedded systems

Huge data centers are increasing the use of GPU and beginning to use FPGAs to implement parallel processing.

Both present flexible architectures with rapid reconfiguration of the elementary processing cores.

The main difference is that GPU consumes much more electric power than FPGA.

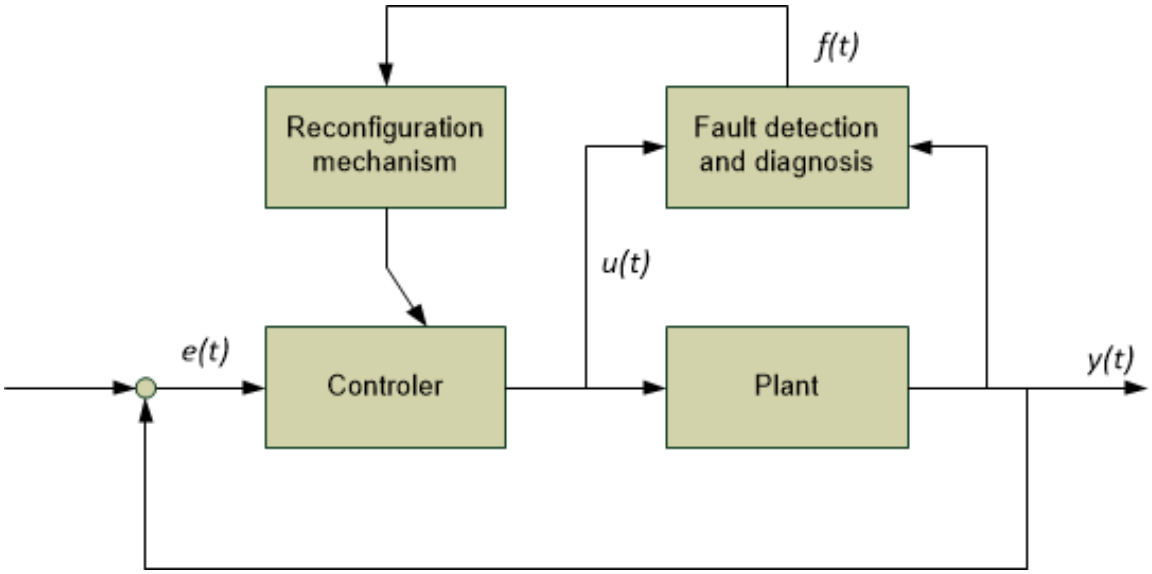
Flexibility and low electric consumption: FPGA is the natural choice for embedded systems.

FPGA parallelism goals

- Architectural studies to provide parallelism to hardware implementation of algorithms, in order to achieve significant performance acceleration.
- New architectures for embedded systems presenting computation power, flexibility, low electrical consume and low overall costs.
- That is the main road for embedded systems in the near future, in order to be able to execute new functionalities.
- It ends up to implementing new FPGA parallel algorithms to get powerful computation in small systems with low electrical consumption.

Reconfigurability

- Fault-tolerant control systems



Digital reconfigurability

- Faults in the digital computation system that are in charge of the controller algorithm.
- Digital system faults: aging, radiation exposure, vibration, short or open circuits, and so on.
- Complex embedded systems need to mix the two frameworks
- Ability to observe and assess every action, event or communication continuously.
- This is a big data problem about a system of systems, which points to sophisticated classification methods.

Supervised machine learning

- Big data diagnostic methods
  - Associative rule-based diagnosis systems (ARB)
  - Support vector machines classifiers (SVM)
  - Convolution neural networks (CNN)

ARB

- Rule-based methods uses rules if *antecedents* are true then *consequents* are true.
- Consequents may be actions or another logical step in a inference chain.
- Data mining methods based on association by correlation between features lead to rule mining methods.
- Parallel techniques are the solution to accelerate the process of rule mining in large hyperspaces.

SVM

- Linear surface separation of clusters may have several solutions.
- SVM finds the maximum margin separation surface.
- For non linear separable problems, a nonlinear transformation can generate another space where a linear separator exists.
- SVM has been applied to several classification problems with great level of success.

CNN

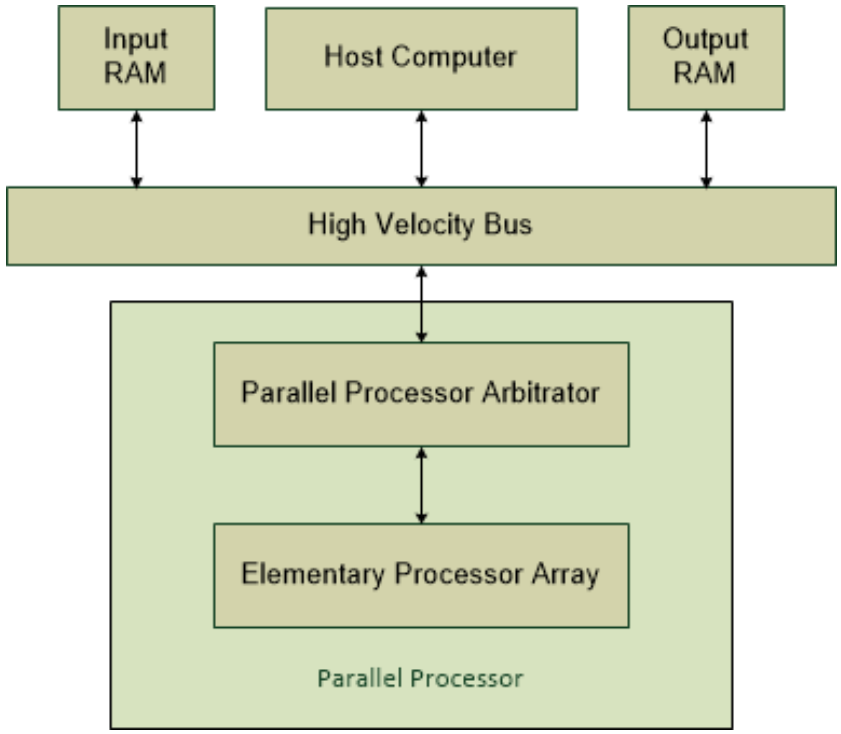
- Neural networks called perceptrons have been used for classification in several applications.
- However it needs in general expert data pre-processing.
- CNN are deep networks that can process raw data.
- Several big data application with great results confirm that CNNs present several advantages over other classification methods.

FPGA

- Recent SoC boards encapsulating together microprocessors and FPGAs gives more flexibility to embedded systems.
- Recently released OpenCL compilators permits standard designs and short worflow given that is based on IPs.
- Reconfiguration can be designed based on parameters to ensure fast response.

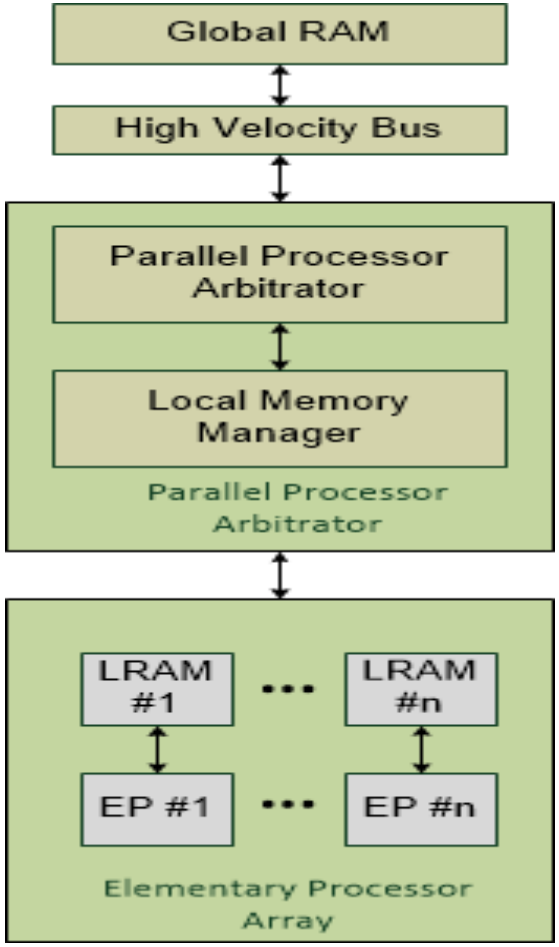
SoC-based Architecture

- SoC: host computer and FPGA



Parallel processor

- Details



Conclusions

- The proposed architecture allows to implement several classification methods reusing the structure and changing only the elementary processors.
- It makes viable to achieve real-time partial reconfigurability to embedded systems.
- Preliminary tests shows 10 times acceleration for a computer vision application of a pedestrian detection in photographs.