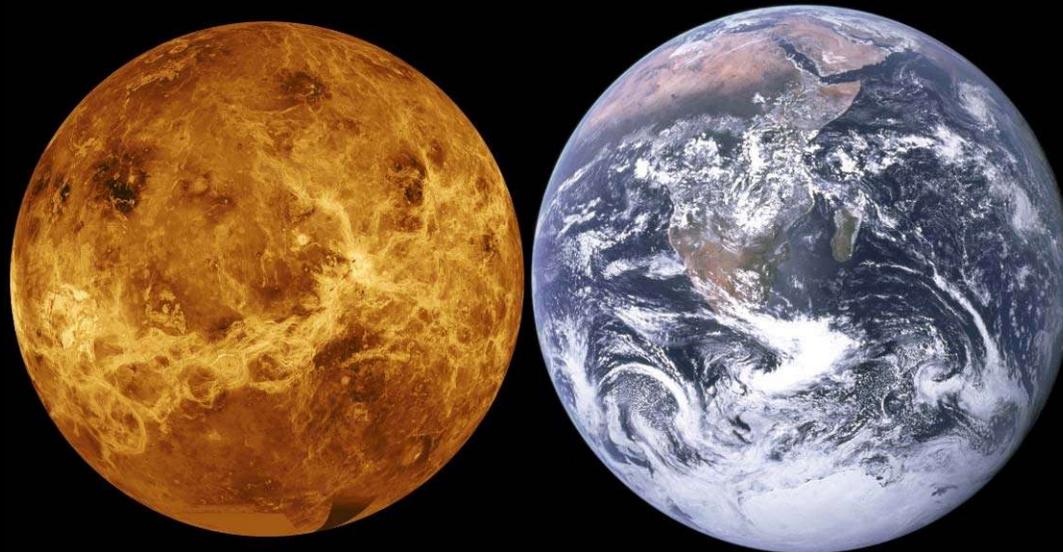




Working on Venus – a Project on Extreme Environment Electronics

Carl-Mikael Zetterling

*Knut and Alice
Wallenberg
Foundation*



www.WorkingonVenus.se



Working on Venus

KAW Funded 2014 – 2018

Carl-Mikael Zetterling AND Mikael Östling,
Christer Fuglesang, B. Gunnar Malm, Hans-Peter Nee,
Frank Niklaus, Ana Rusu, [Anita Lloyd Spetz](#)
[Mike Andersson](#), Per-Erik Hellström, Saul Rodriguez
Juan Colmenares, Mattias Ekström, Hossein Elahipanah,
Shuoben Hou, [Lida Khajavizadeh](#), Miku Laakso, Muhammad
Shakir, Ye Tian, Muhammad Waqar Hussain
KTH and [Linköping University](#)



Working on Venus 2014 - 2018

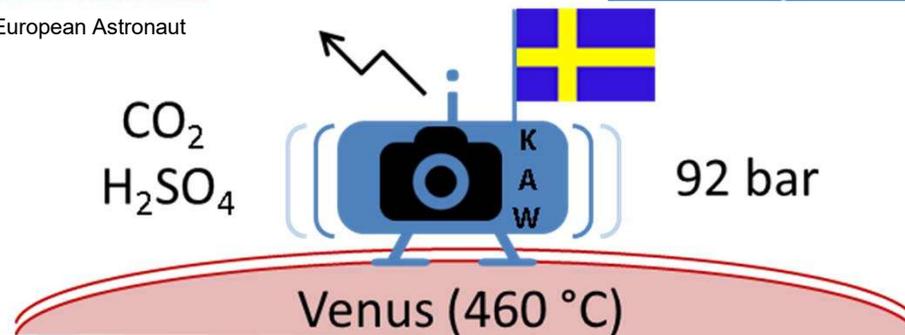
Knut and Alice Wallenberg Foundation

www.WorkingonVenus.se

Prof. Christer Fuglesang



European Astronaut



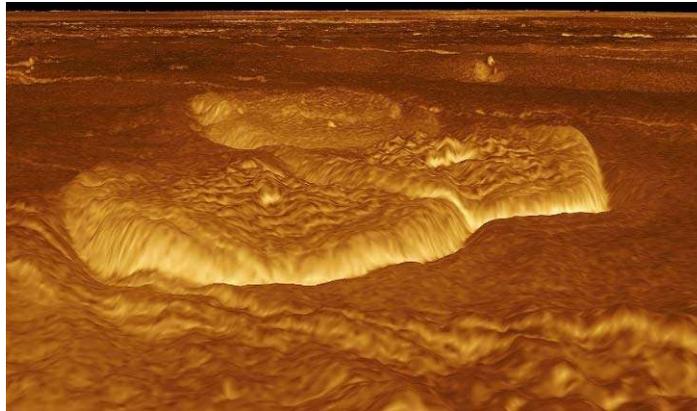
www.WorkingonVenus.se

Venus Atmosphere

96% CO₂ (Also sulphuric acids)

Pressure of 92 bar (equivalent to 1000 m water)

Temperature 460 °C



From Wikimedia Commons, the free media repository

- Difficult to explore
- Life is not likely

Previous Missions



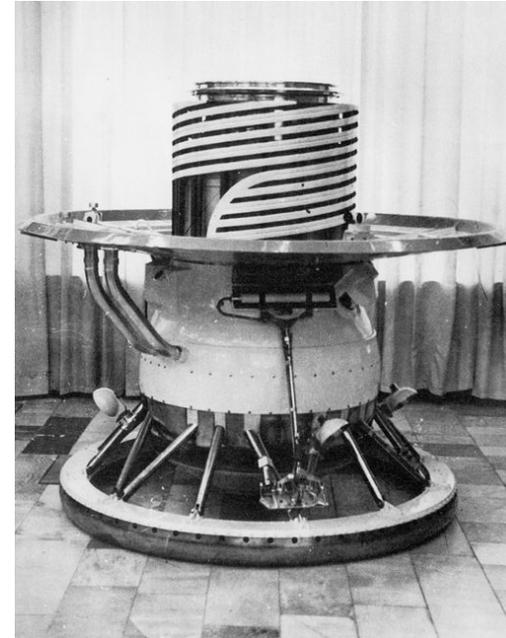
From Wikimedia Commons, the free media repository

Venera 1 – 16 (1961 – 1983) USSR
Mariner 2 (1962) NASA, USA
Pioneer (1978 – 1992) NASA, USA
Magellan (1989) NASA, USA
Venus Express (2005 -) ESA, Europa
Akatsuki (2010) JAXA, Japan

Venera 9 and 10 (1975)



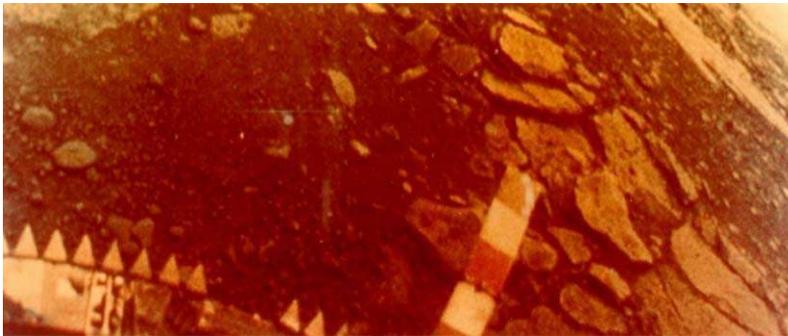
From Wikimedia Commons, the free media repository



From Wikimedia Commons, the free media repository

Electronics functional around 1 hour
First B/W images

Venera 13 and 14 (1981)



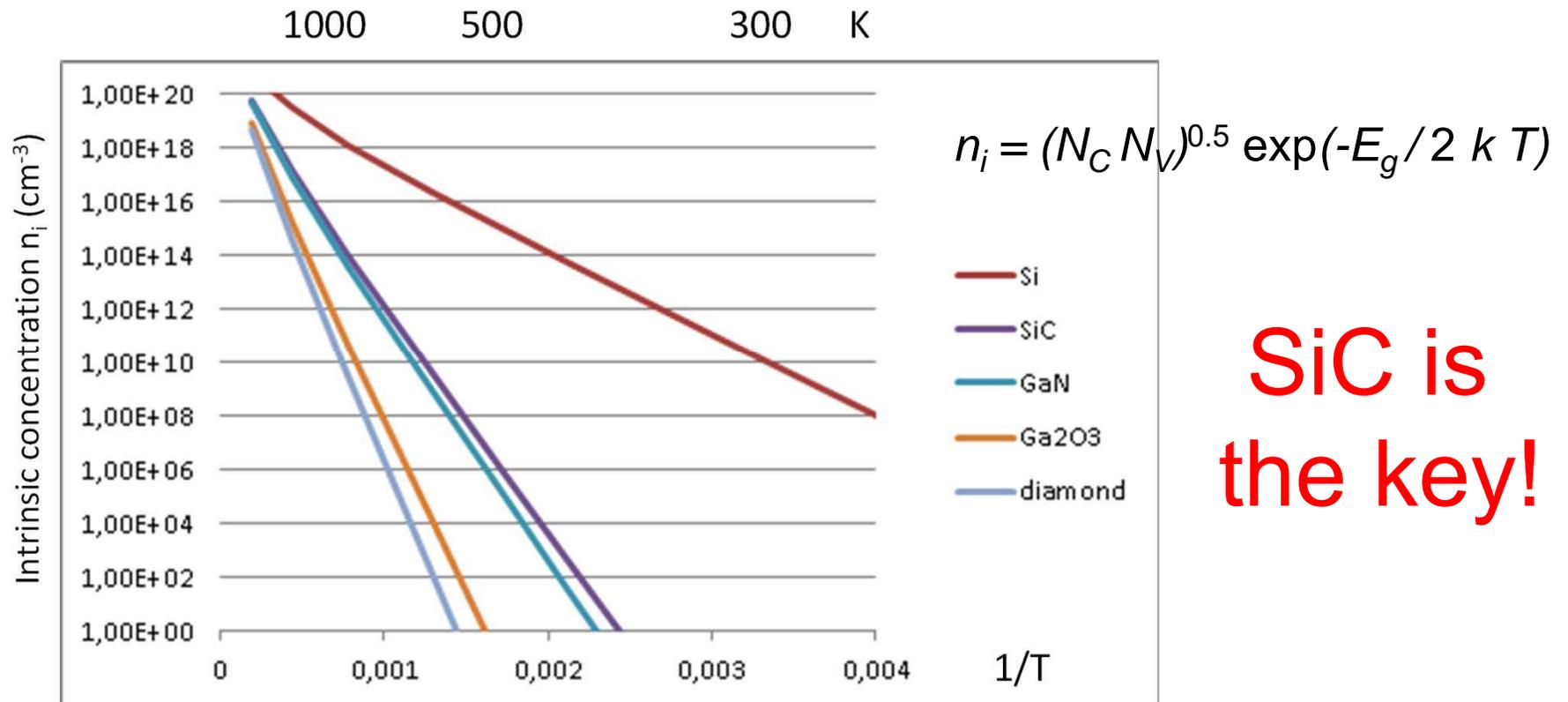
From Wikimedia Commons, the free media repository



From Wikimedia Commons, the free media repository

Electronics functional around 2 hours
First color images
No signs of life

Intrinsic Concentration vs Temperature



SiC is the key!



NASA Glenn test chamber mimics Venus' harsh conditions ("Hell on Earth")



NASA Glenn aerospace engineer Rodger Dyson shows one of the 100-pound bolts that will secure the lid of the new extreme environments test chamber.

http://www.cleveland.com/science/index.ssf/2012/06/new_test_chamber_at_clevelands.html
<http://www.wired.com/2012/01/nasa-venus-chamber/>

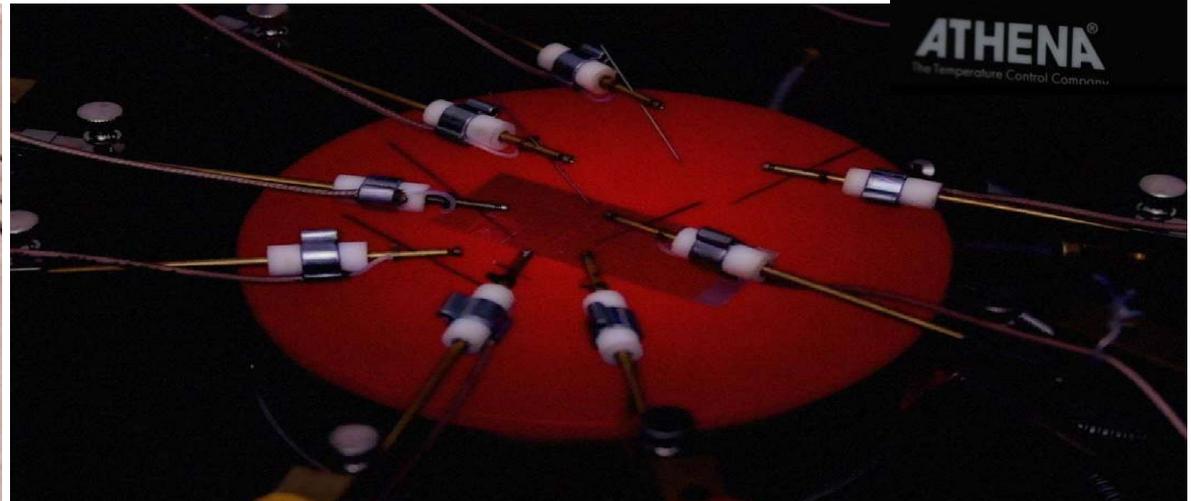
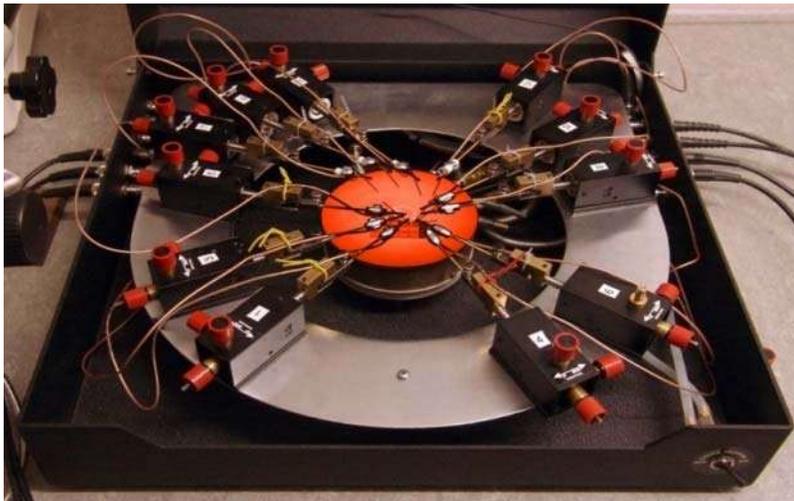


Testing facilities for electrical characterization

On wafer probing up to 620 °C

Parameter analyzer for DC characteristics

Digital oscilloscope/FFT for AC characteristics



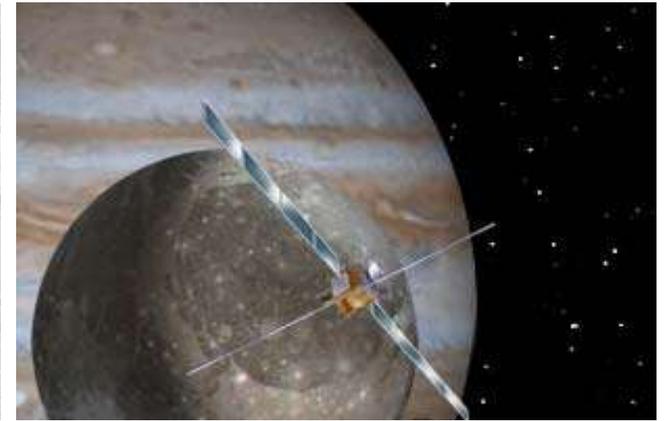
And beyond Venus...



Fukushima

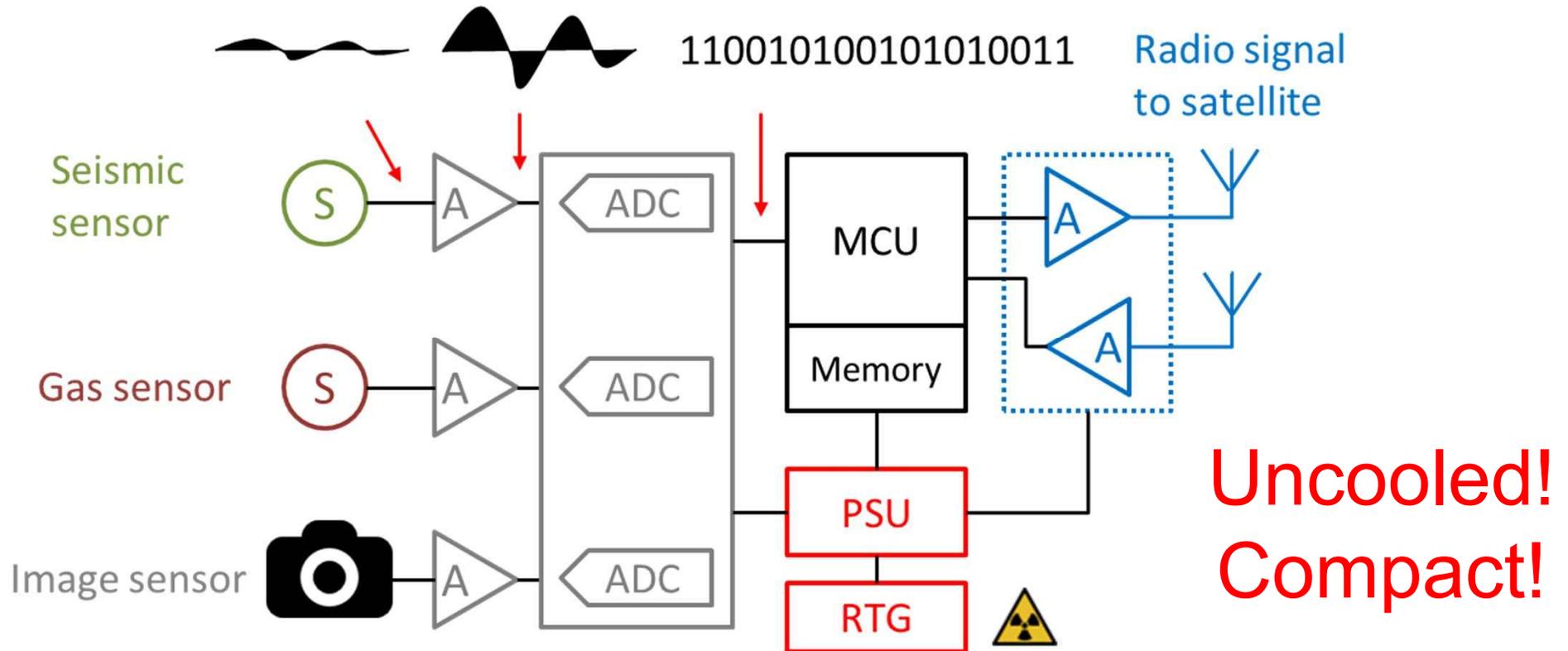


Shinkansen N700s



Jupiter Moons mission
(JUICE)

Working on Venus – Lander Block Diagram





Cleanroom for IC and Device Fabrication

Electrum Laboratory 1300 m²

ISO 9001 certified / controlled processes
and calibrated characterization tools

100 – 200 mm wafers

Silicon Technology

Silicon - IC

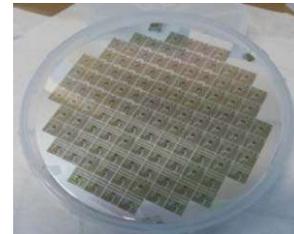
Silicon - Microsystems

Compound Semiconductors

SiC – Electronics, 100 mm

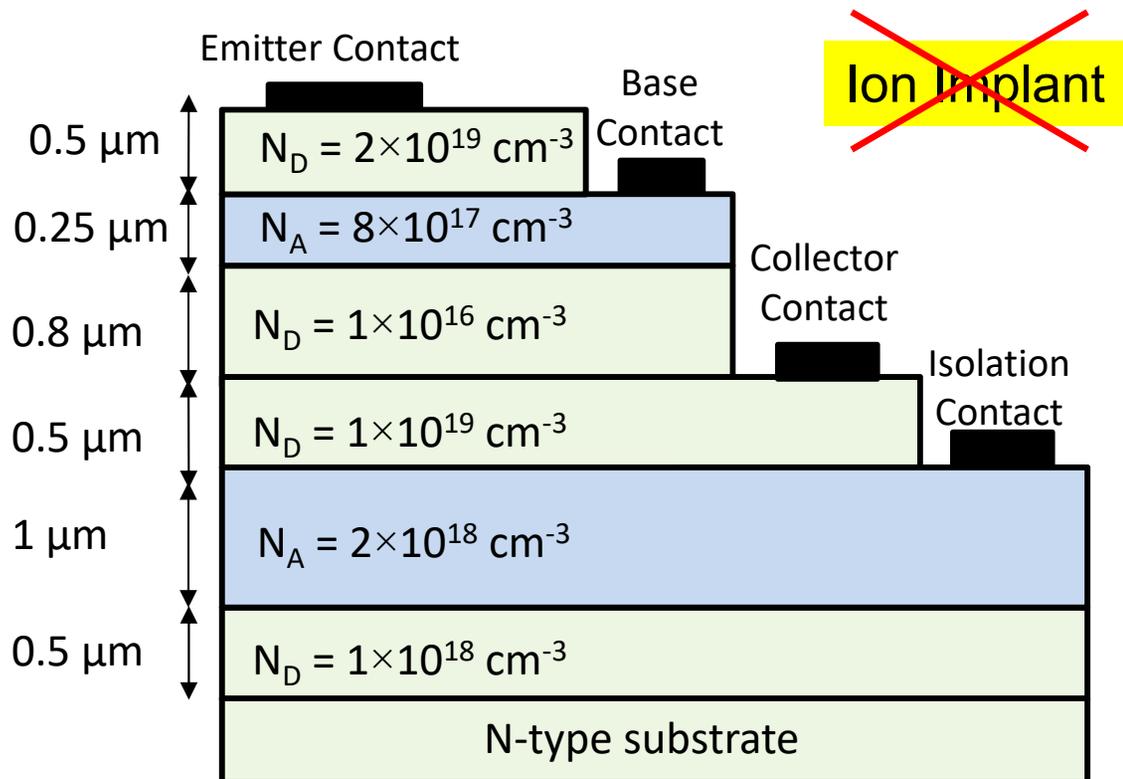
InP - Opto / electronics

GaAs - Opto / electronics



Part of  - the Swedish national research infrastructure for micro- and nanofabrication

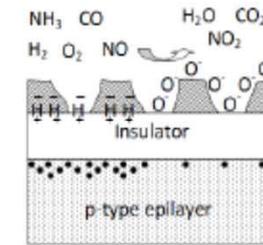
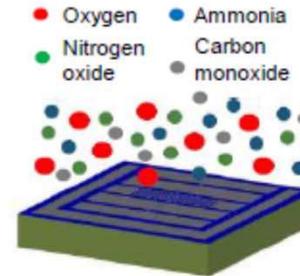
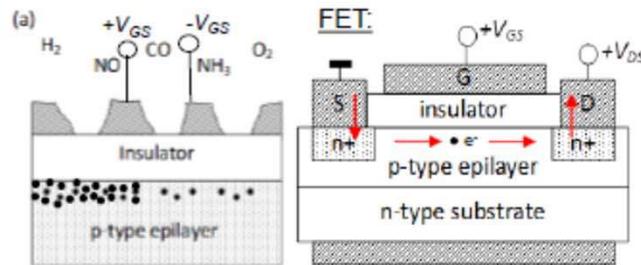
Bipolar Process Technology



- SiC Dry Etching
 - Reactive Ion Etching
- Sacrificial Oxidation
 - 1100 °C, 3 hours, in O₂
- Passivation Oxidation
 - 1250 °C, 3 hours, in N₂O
- Contact Salicide
 - Ni, 600 °C, 1 min
- N-type Ohmic Contact
 - 950 °C, 1 min
- P-type Ohmic Contact
 - Ti/Al deposition, patterning and etching
 - > 900 °C, 1 min
- TiW/Al Metal Interconnects

Field Effect Transistor Gas Sensors

(High-temperature operation, 500 °C)

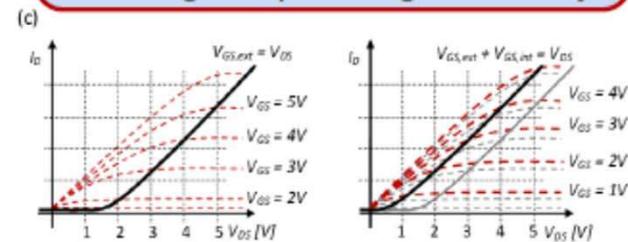
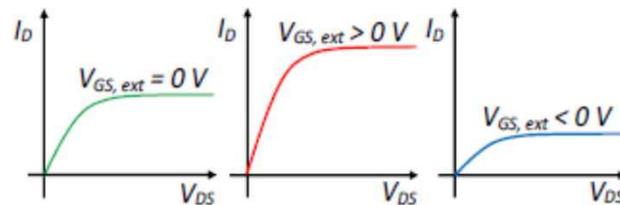


Each sensor chip contains at least one field effect transistor (FET)

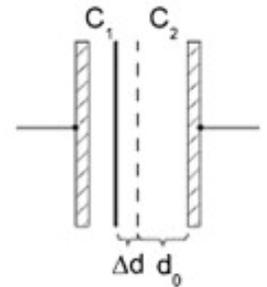
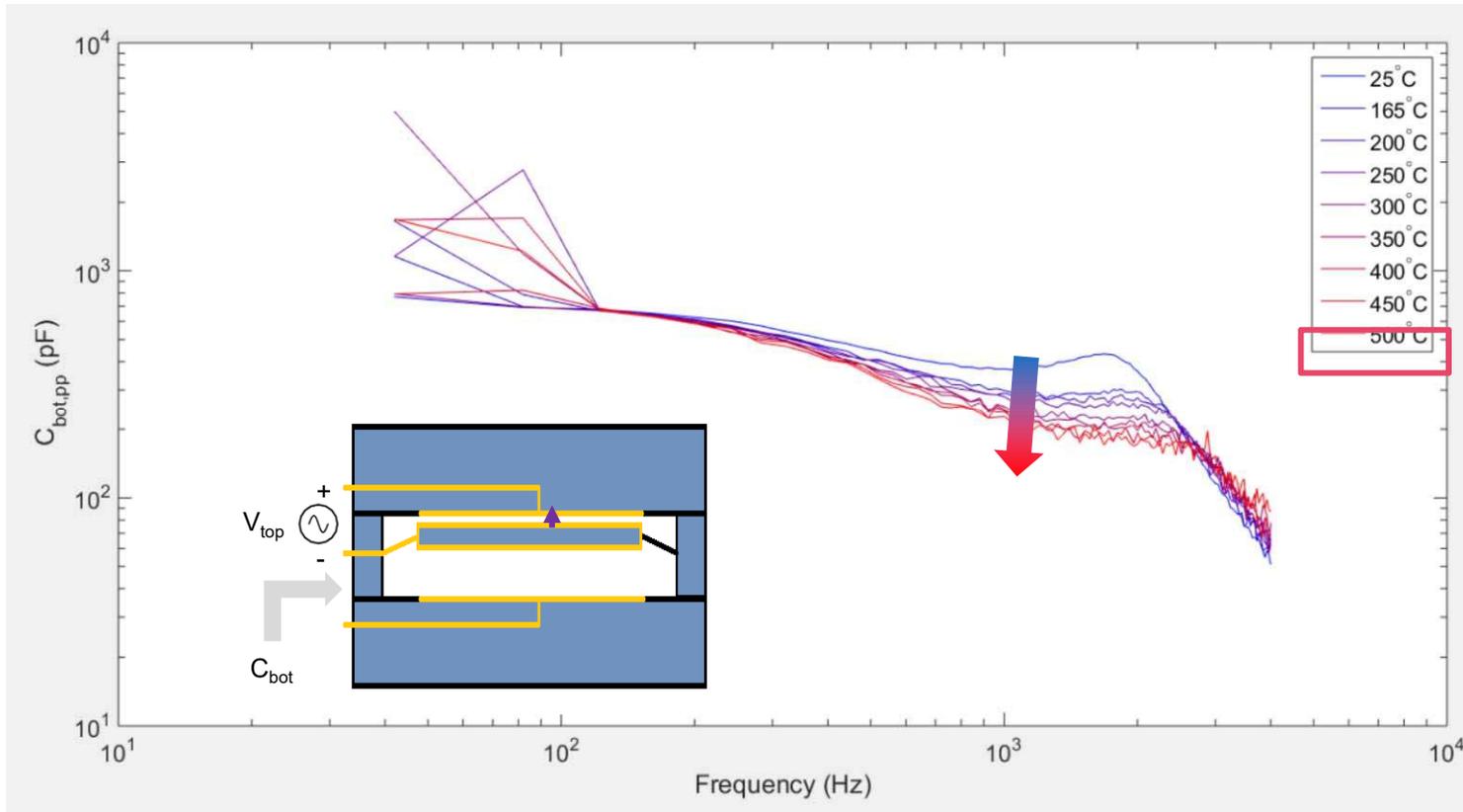
The voltage, $V_{GS,ext}$, applied to the gate, G, determines the drain current, I_D , through the transistor

Certain gas species change the gate voltage (by $V_{GS,int}$) when adsorbing on the gate, altering the I/V-characteristics

High-temperature operation requires:
1) Reliable metallization/ Ohmic contacts, 2) Gate material stability, 3) Good high-temperature gas sensitivity

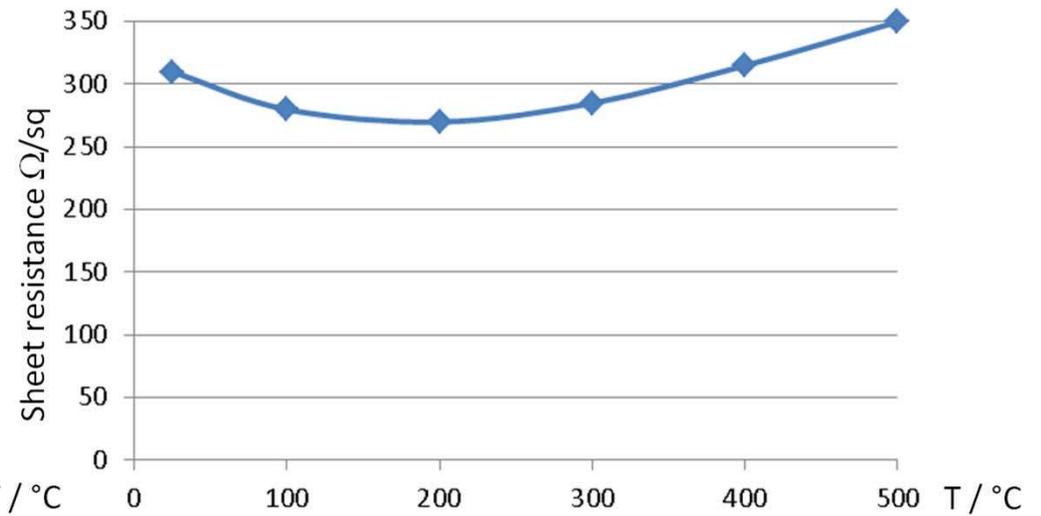
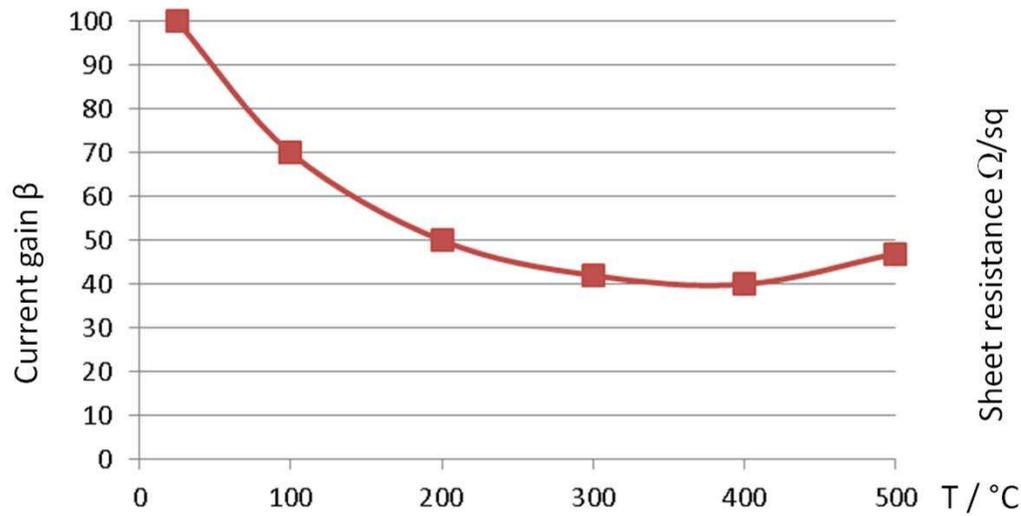


Accelerometer – Frequency response

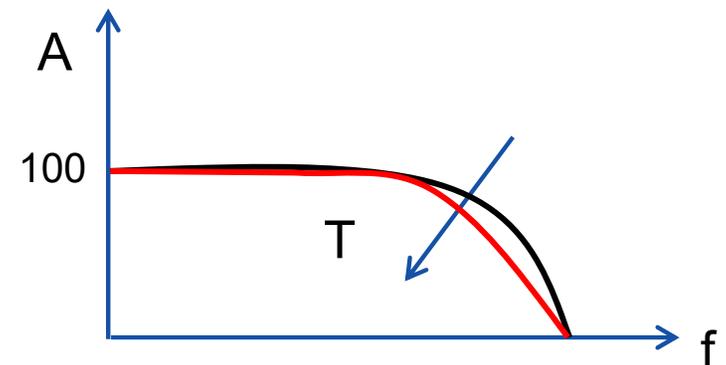
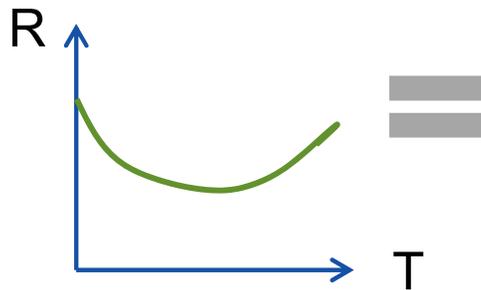
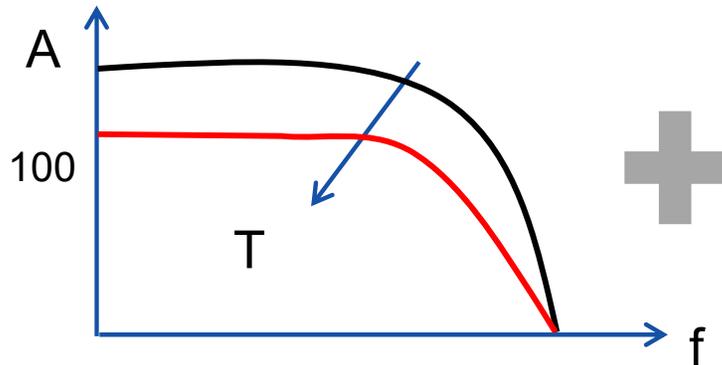
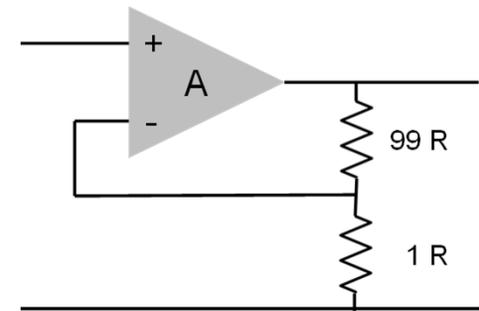
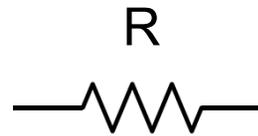
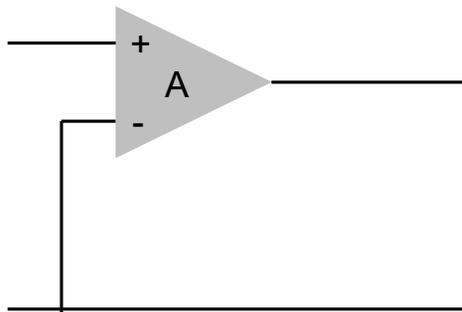




Current gain and sheet resistance



Negative Feedback for Analog circuits





SiC Amplifiers

Material aspects of wide temperature range amplifier design in SiC bipolar technologies

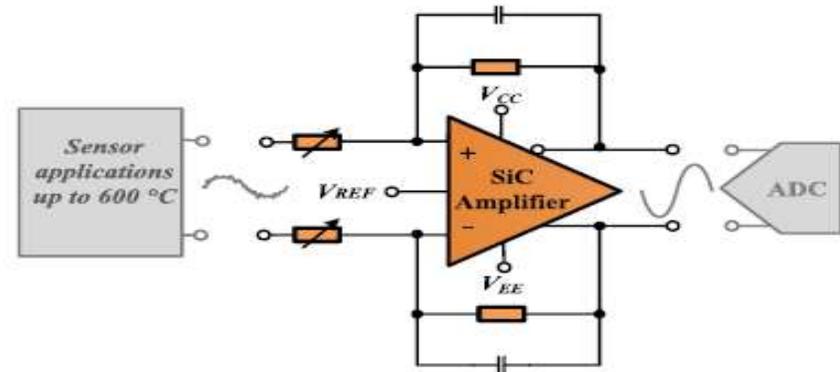
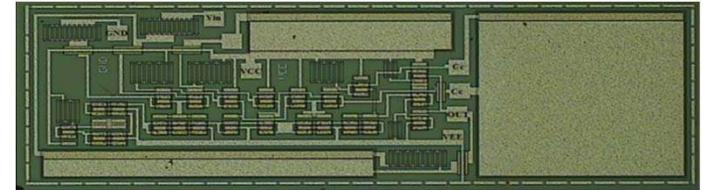
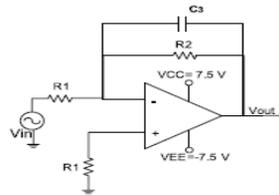
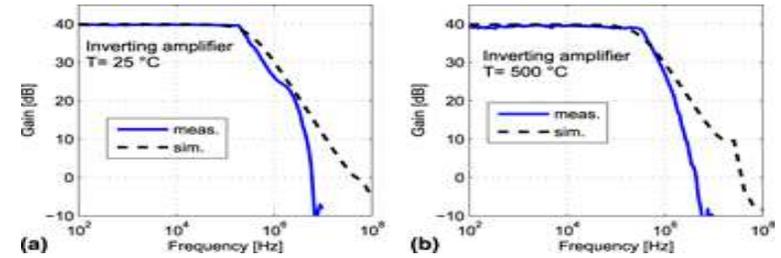
R. Hedayati et al. J. Materials Research 31 (2016) 2928 – 2935 DOI: 10.1557/jmr.2016.321

A monolithic, 500 °C operational amplifier in 4H-SiC bipolar technology

R. Hedayati et al. IEEE Electron Dev. Lett. 35 (2014) 693-695 DOI: 10.1109/LED.2014.2322335

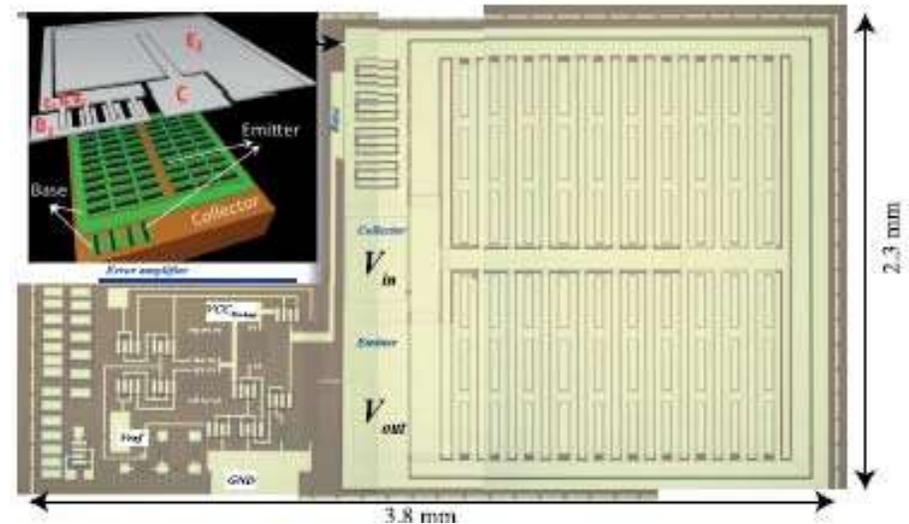
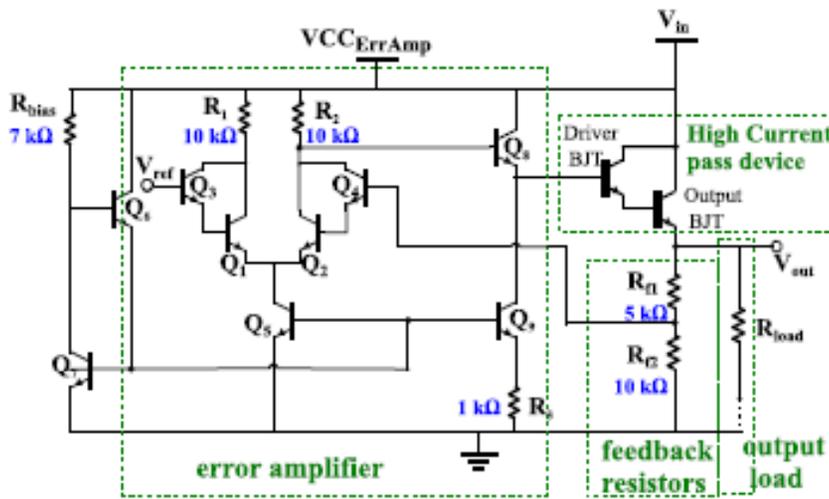
Silicon carbide fully differential amplifier characterized up to 500 °C

Y. Tian et al. IEEE Trans. Electron Dev. 63 (2016) 2242 – 2247 DOI: 10.1109/TED.2016.2549062



2 A Linear Voltage Regulator

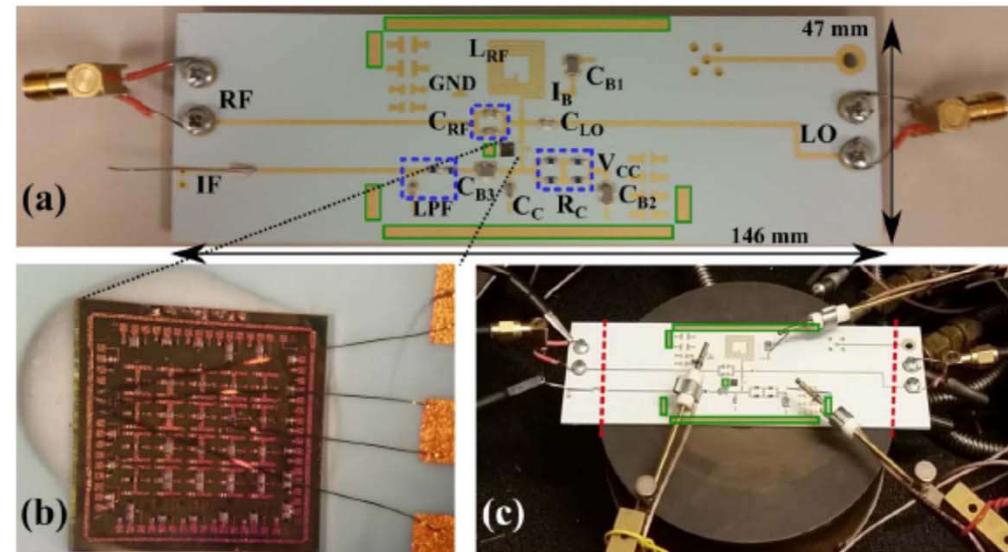
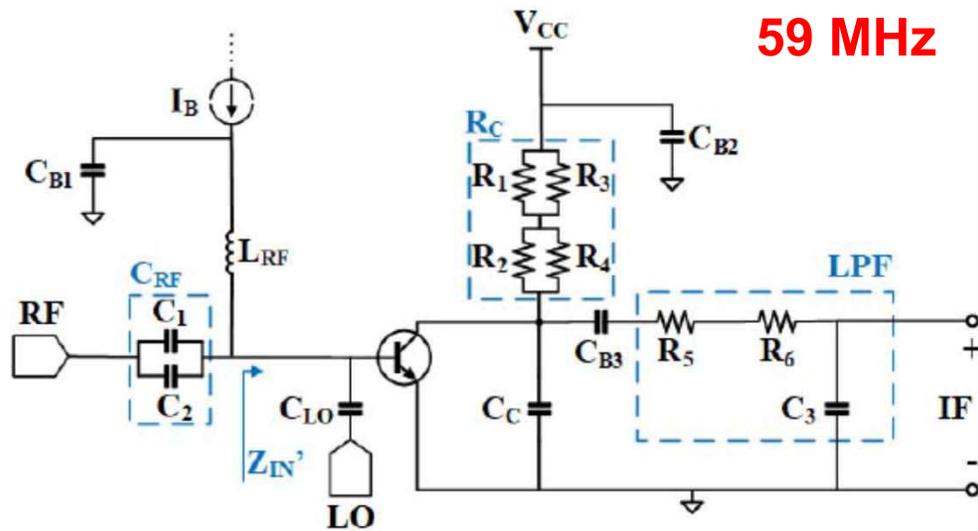
500 °C, High Current Linear Voltage Regulator in 4H-SiC BJT Technology,
 S. Kargarrazi et al., IEEE Electron Device Letters, vol. 39, p. 548, 2018.
 DOI: 10.1109/LED.2018.2805229



SiC HT Radio Circuits – A challenge to measure

500 °C on chuck but max 200 °C at SMA contacts required LTCC hybrid board for characterization

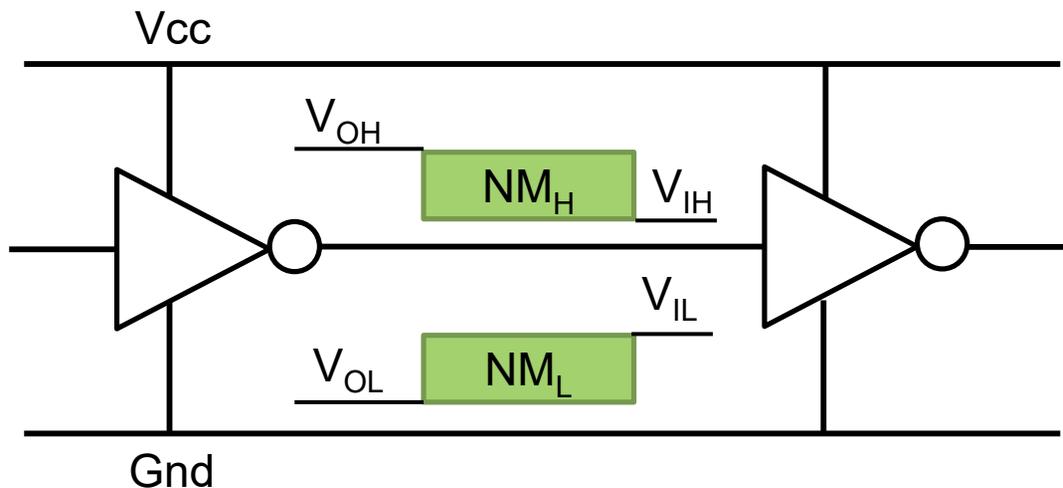
A 500 °C Active Down-Conversion Mixer in Silicon Carbide Bipolar Technology,
M. W. Hussain et al., IEEE Electron Device Letters, Vol. 39, p. 855, 2018.
DOI: 10.1109/LED.2018.2829628



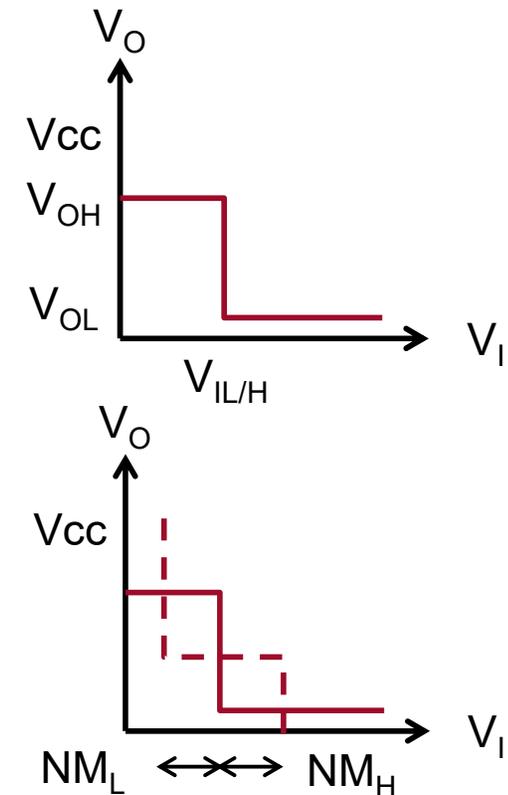
An Intermediate Frequency Amplifier for High-Temperature Applications,
 M. W. Hussain et al., IEEE Trans. Electron Devices, vol. 65, p. 1411, 2018.
 DOI: 10.1109/TED.2018.2804392 (55 MHz, 250 °C)

Noise Margins for Digital circuits

Needs to be measured at every temperature



Electrical Characterization of Integrated 2-input TTL NAND Gate at Elevated Temperature, Fabricated in Bipolar SiC-Technology
M. Shakir et al. ICSCRM 2017

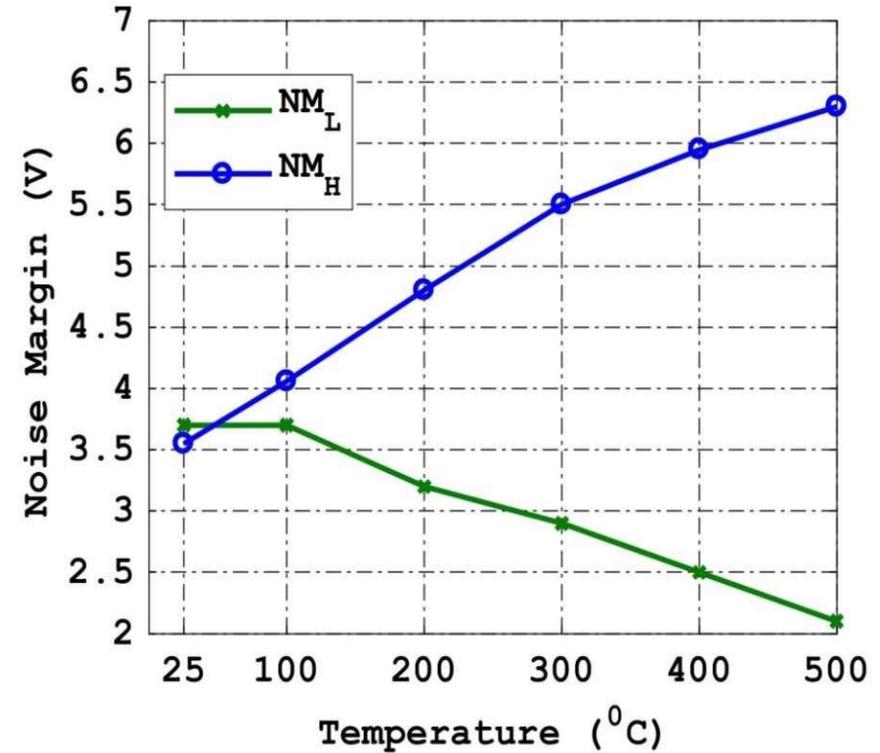
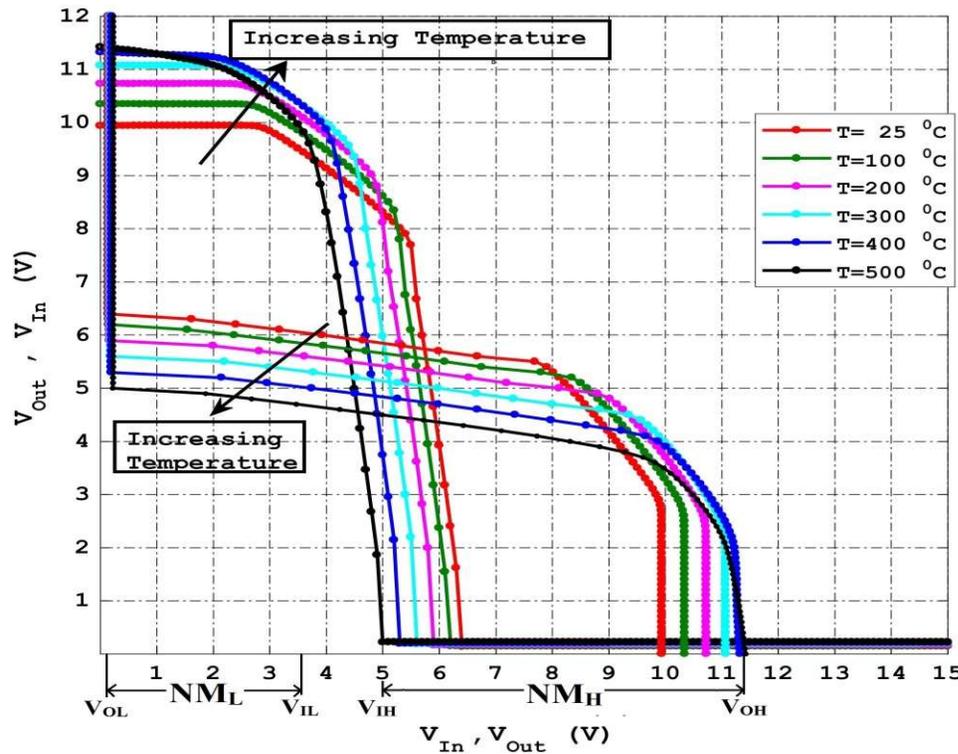


2-input NAND Gate DC-Response at 15 V

VTC vs T

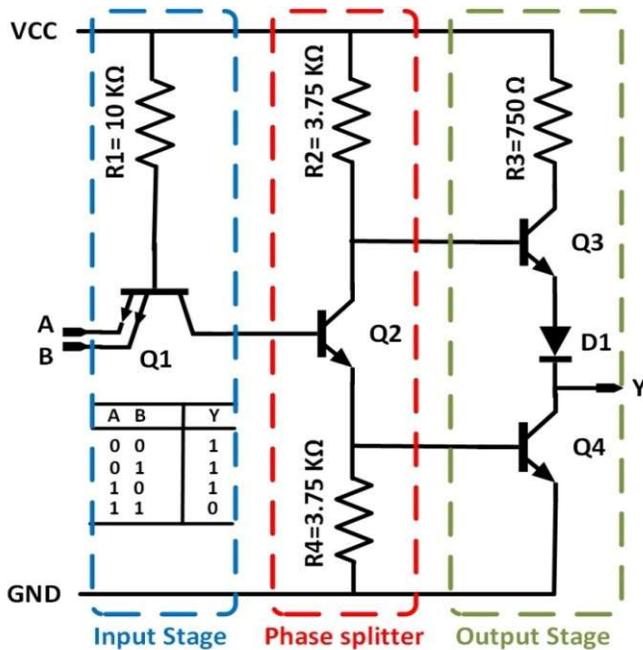
Now also 600 °C operation

NM vs T

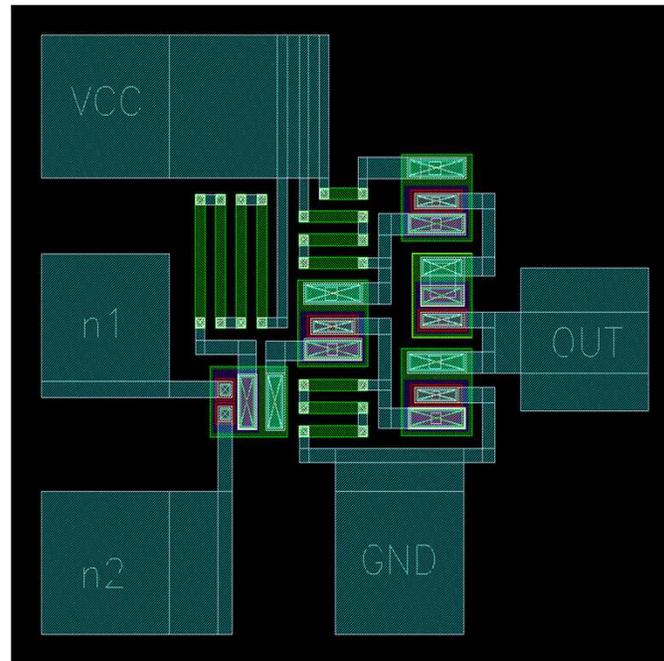


2-input TTL NAND Gate Layout and Micrograph

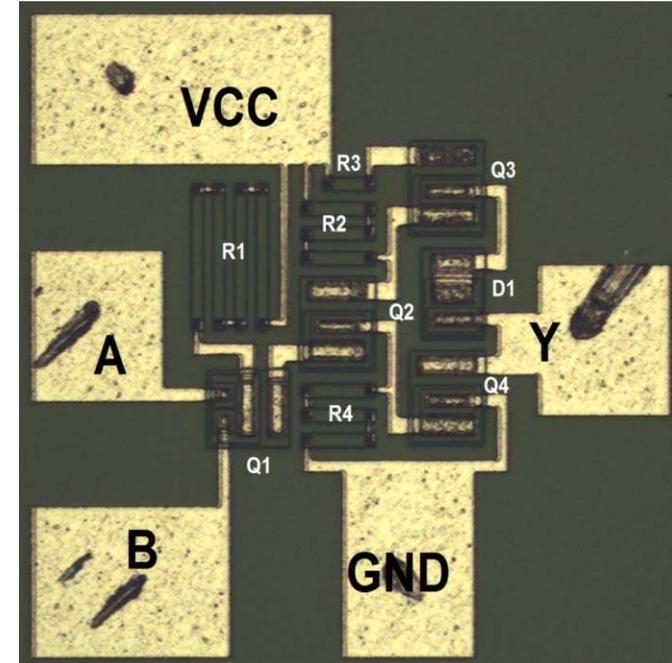
Schematic



Layout



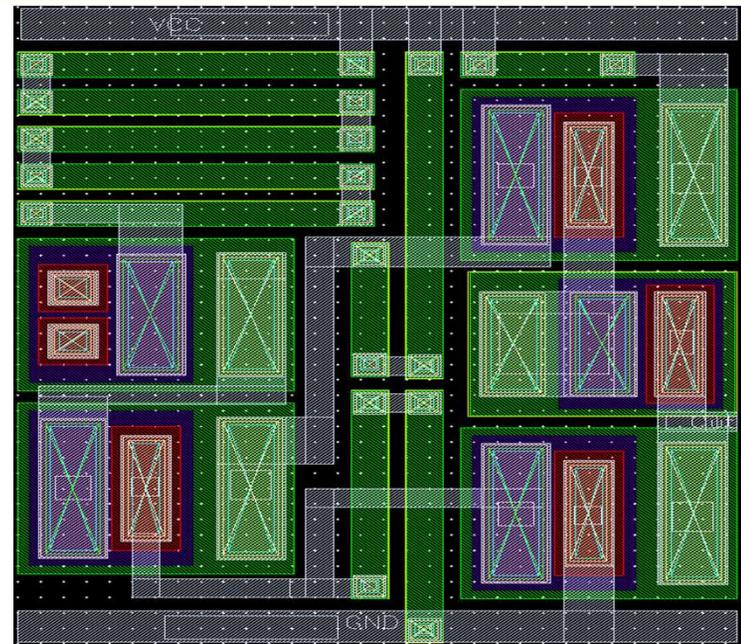
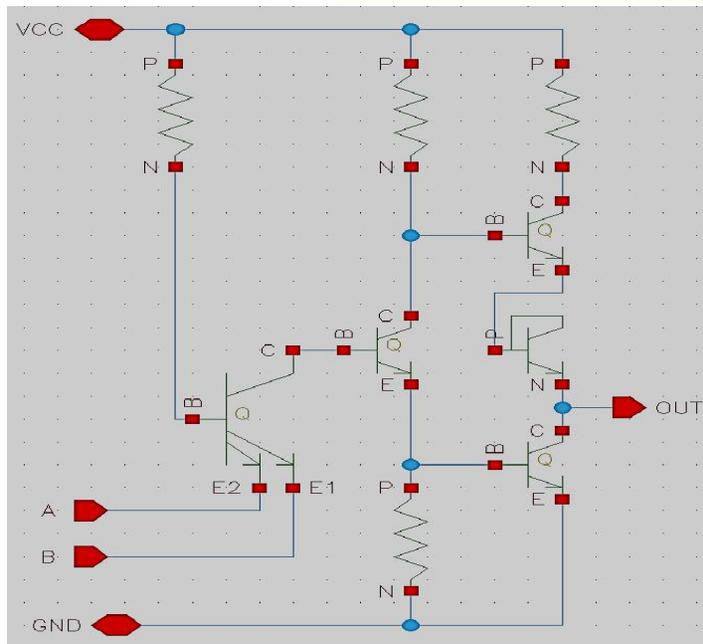
Micrograph



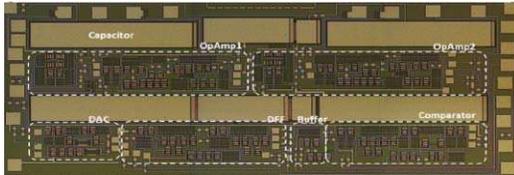
Process Design Kit for TTL gate library

LVS - Layout vs Schematic
DRC / Design Rule Check
Hierarchical gate library

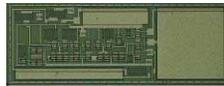
Towards Silicon Carbide VLSI Circuits for Extreme Environment Applications, M. Shakir et al. Electronics 2019 8 (2019) 496
DOI:10.3390/electronics8050496



Next steps



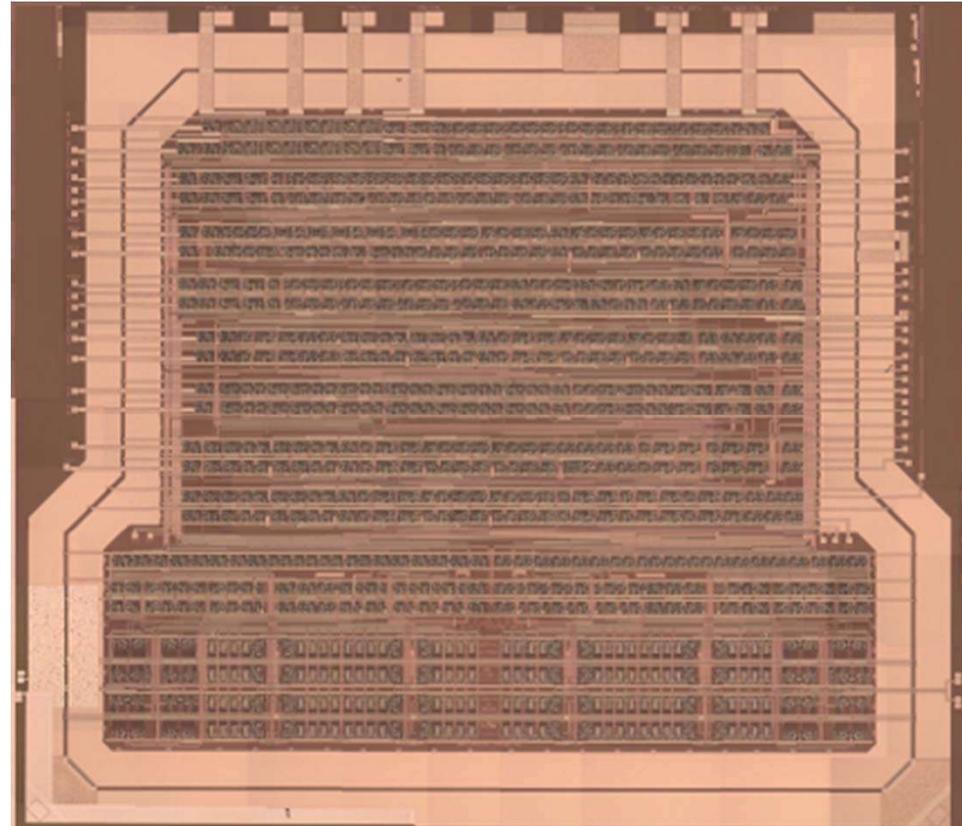
ADC 100 transistors



Amplifier 25 transistors



Logic gate 5 transistors



Microcontroller 6 000 transistors



4 bit TTL CPU

11.4 mm X 13.2 mm = 151 mm²

BJTs = 5911

Integrated Resistors = 3918

V_{cc} = 15 V, 1 A

2 metal layers

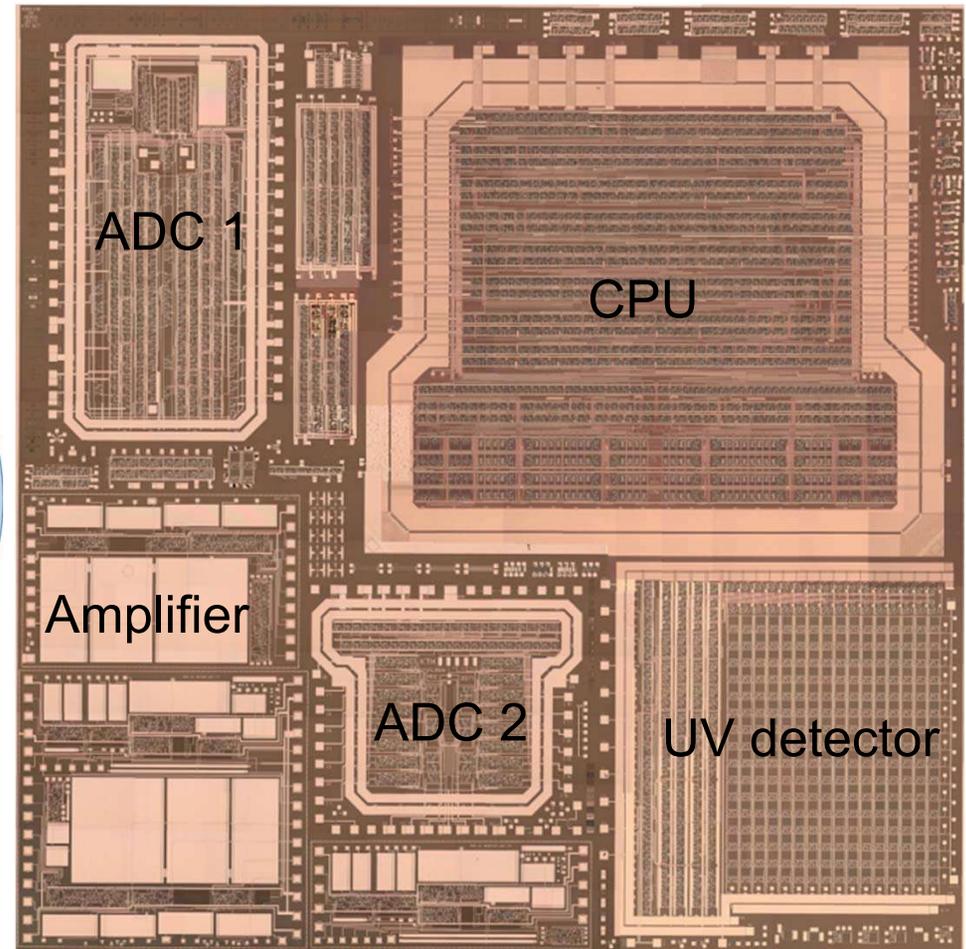
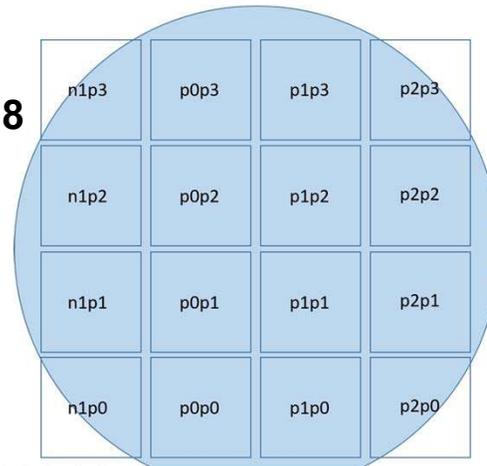
LVS and DRC

Simulated in Spice

Parts characterized up to 600 °C

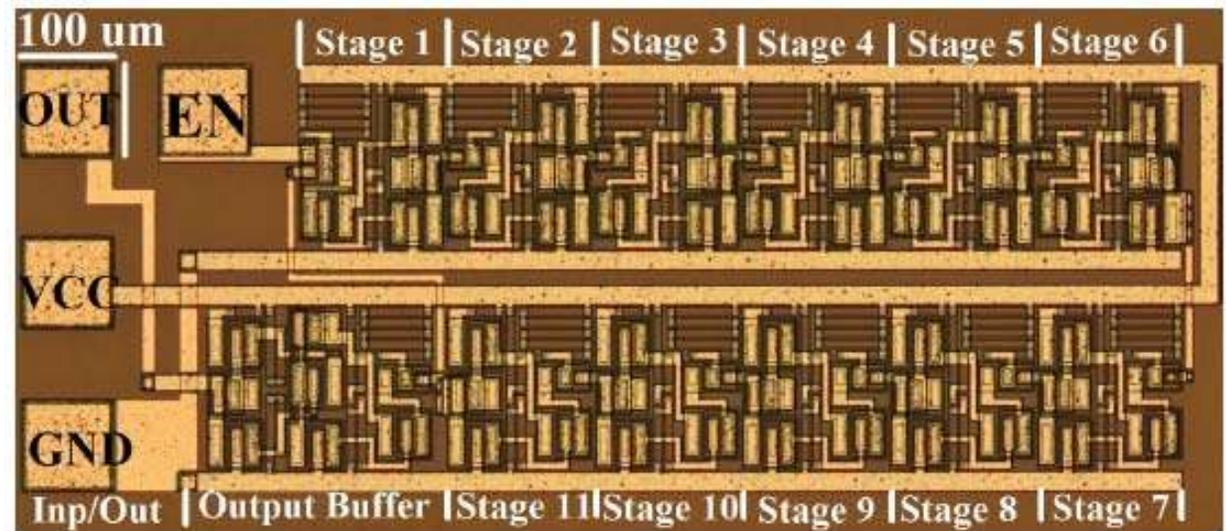
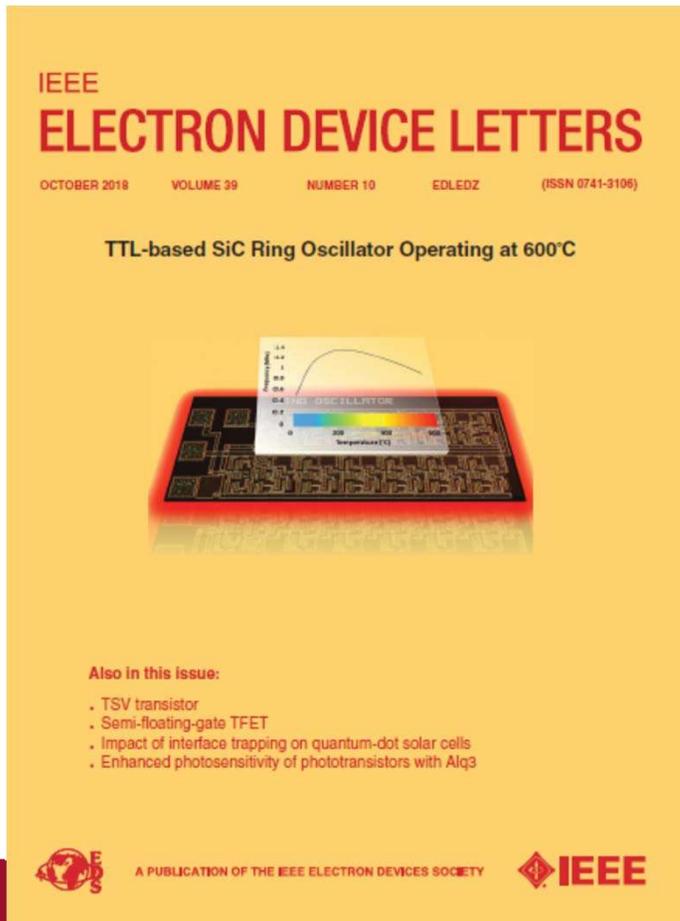
Test chip also contains ADCs,

Amplifiers and UV pixel detector





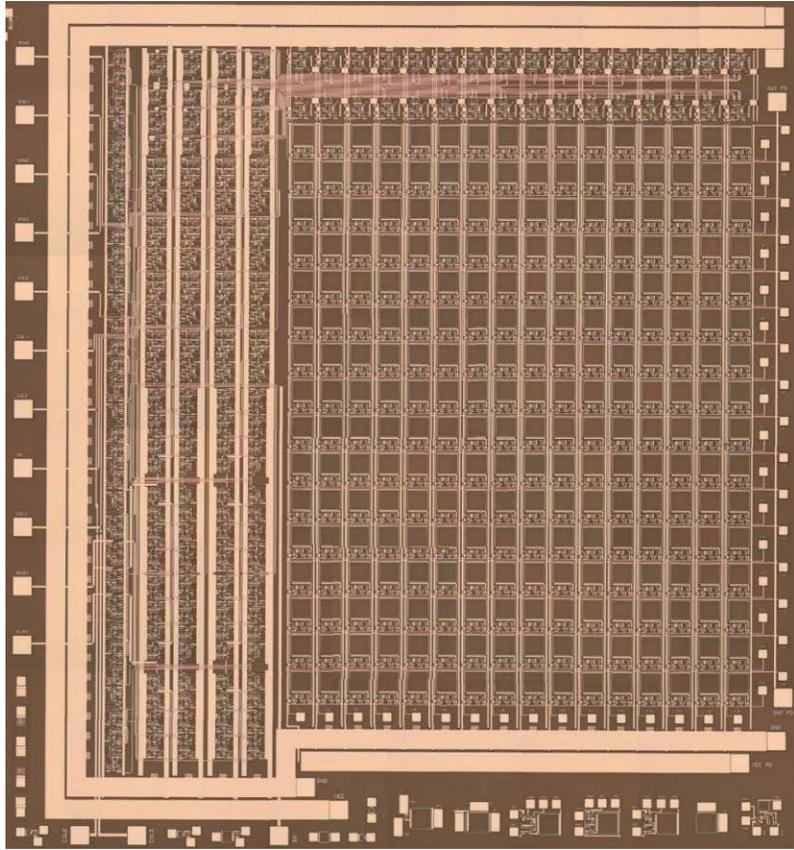
A 600 °C TTL-based 11-stage Ring Oscillator in Bipolar Silicon Carbide Technology



120 devices

M. Shakir et al, IEEE Electron Device Letters, vol 39, p 1540, 2018

Fabricated Image Sensor



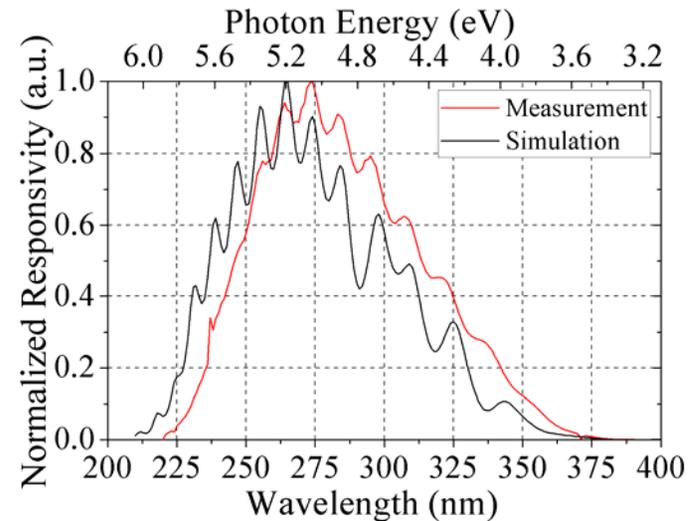
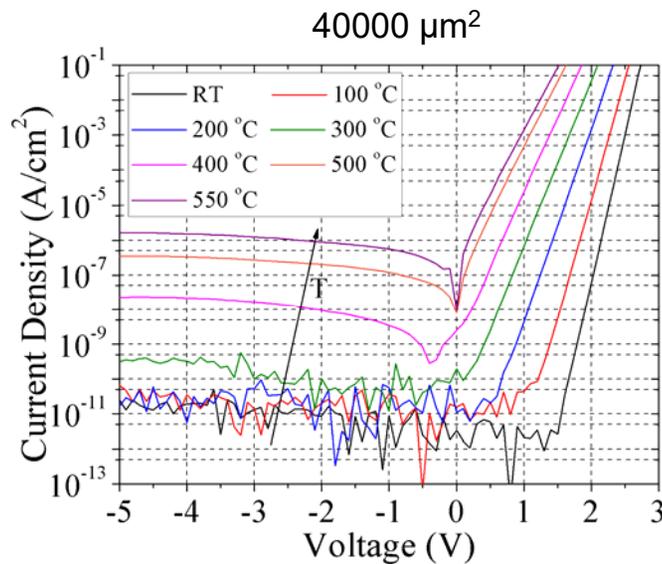
Row 1
Row 2
Row 3
Row 4
Col 1
Col 2
Col 3
Enable
Col 4
Reset
Clock
VCC
Logic

GND
OUT

- Schematic and Layout of the digital circuits are from collaborator contributed TTL PDK
- Two 4-to-16 decoders
- One 8-bit counter
- 16x16 pixels
- 1959 transistors
- 68.2 mm²
- Dynamic mode - 7 I/Os
- Static mode – 13 I/Os

VCC
Sensor

Leakage (Dark) Current and optical response of the SiC Photodiodes



- Leakage current density increases at higher temperatures, but it is still low ($\sim 1 \mu\text{A}/\text{cm}^2$) even at $550 \text{ }^\circ\text{C}$.
- Leakage current density is higher for smaller devices because of surface recombination effect.

Scaling and Modeling of High Temperature 4H-SiC p-i-n Photodiodes, S. Hou et al., *IEEE Journal of the Electron Devices Society*, 6 (1), pp. 139-145, 2018.



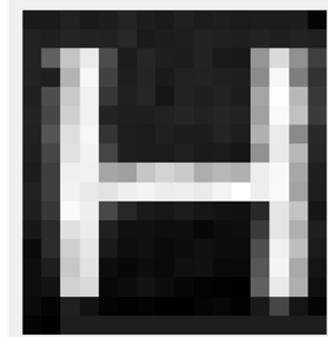
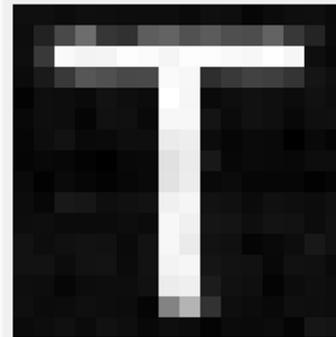
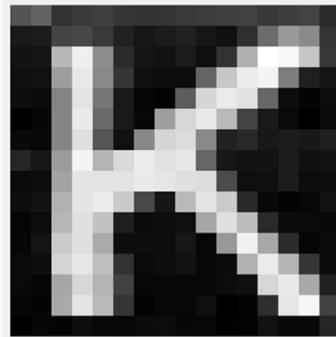
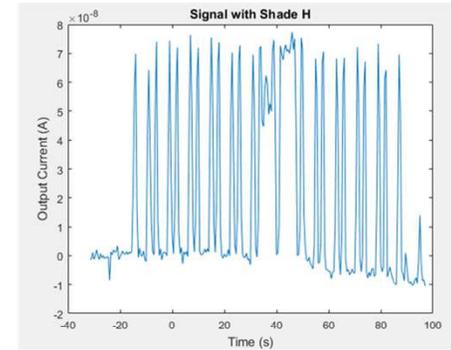
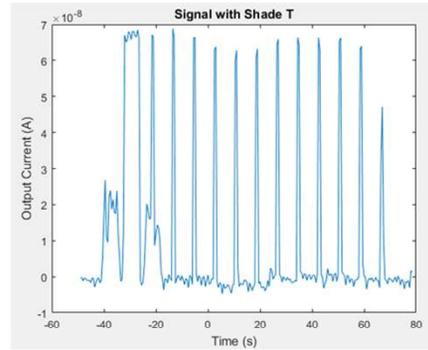
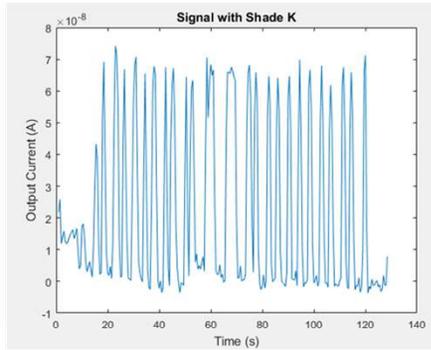
Pixel detector in operation

RT

K

T

H



Ferroelectrics for NVRAM (below 660 °C)

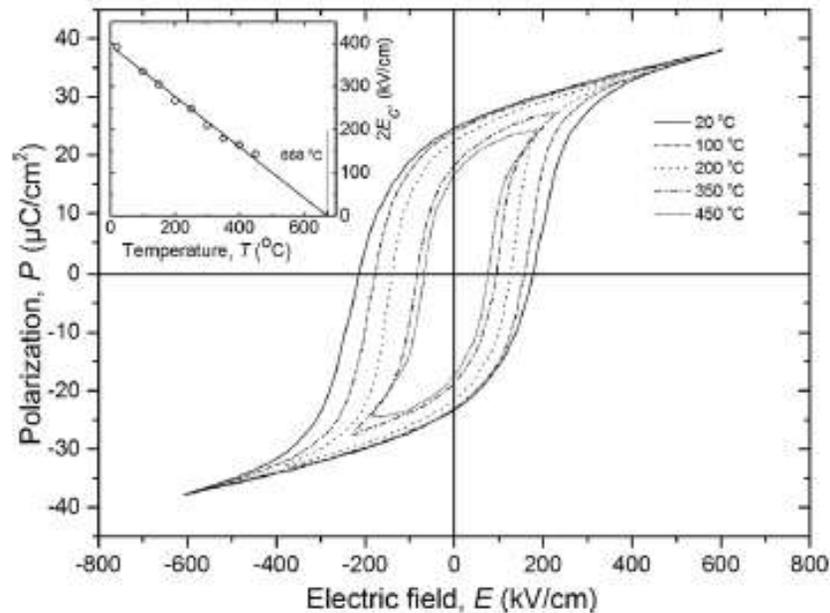
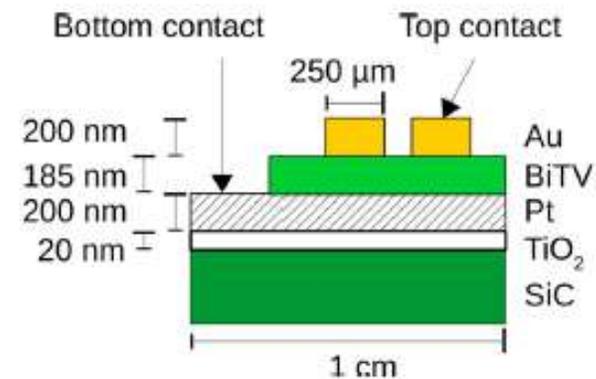


Fig. 9. Hysteresis loop at several different temperatures. Both the coercive field and polarization decrease with increasing temperature. The inset shows the coercive field versus temperature.



Integration and high-temperature characterization of ferroelectric Vanadium-doped Bismuth Titanate thin films on Silicon Carbide

M. Ekström et al. J. Electronic Materials, 2017
DOI: 10.1007/s11664-017-5447-3



Working on Venus - PhD defenses (7+2)

Juan Colmenares – SiC Power Circuits, 2016

Hossein Elahipanah – HV and HT transistors, 2017

Ye Tian – Readout circuitry for accelerometer, 2017

Shuoben Hou – UV photodetectors (16 x 16 bit array), 2019

Mattias Ekström – CMOS and memory devices, 2019

Muhammad Waqar – RF circuits, 2019

Muhammad Shakir – Process Design Kit for digital ASICs, 2019

Miku Laakso – Accelerometer integration, TBD

Lida Khajavizadeh – Gas Sensors, TBD



Summary and outlook

- Bipolar integrated circuits in SiC can handle 500 °C
- Sensors, Amplifiers, Analog-to-Digital Converters, Microcontrollers, Memory, Radio Transceiver and Power Supply demonstrated (on Earth)
- **5 000+ device level fabricated and tested**
- 100 000 device level **systems** possible for Venus Lander

Acknowledgements

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